Event Time stamping architectures of proposed ASICs for position and energy measurements using various detectors at some FAIR experiments.

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OUTLINE

- Architecture of *_XYTER Chips (MSGCROC, N_XYTER).
  - Timing channel
  - Energy channel
- Test setup
- Some test results.
- Conclusions.
- CBM_STS Targeted Specifications…

  … and perhaps ASIC for other FAIR experiments

Position - X, Y, Time and Energy Readout Electronics (XYTER VLSI ASIC)

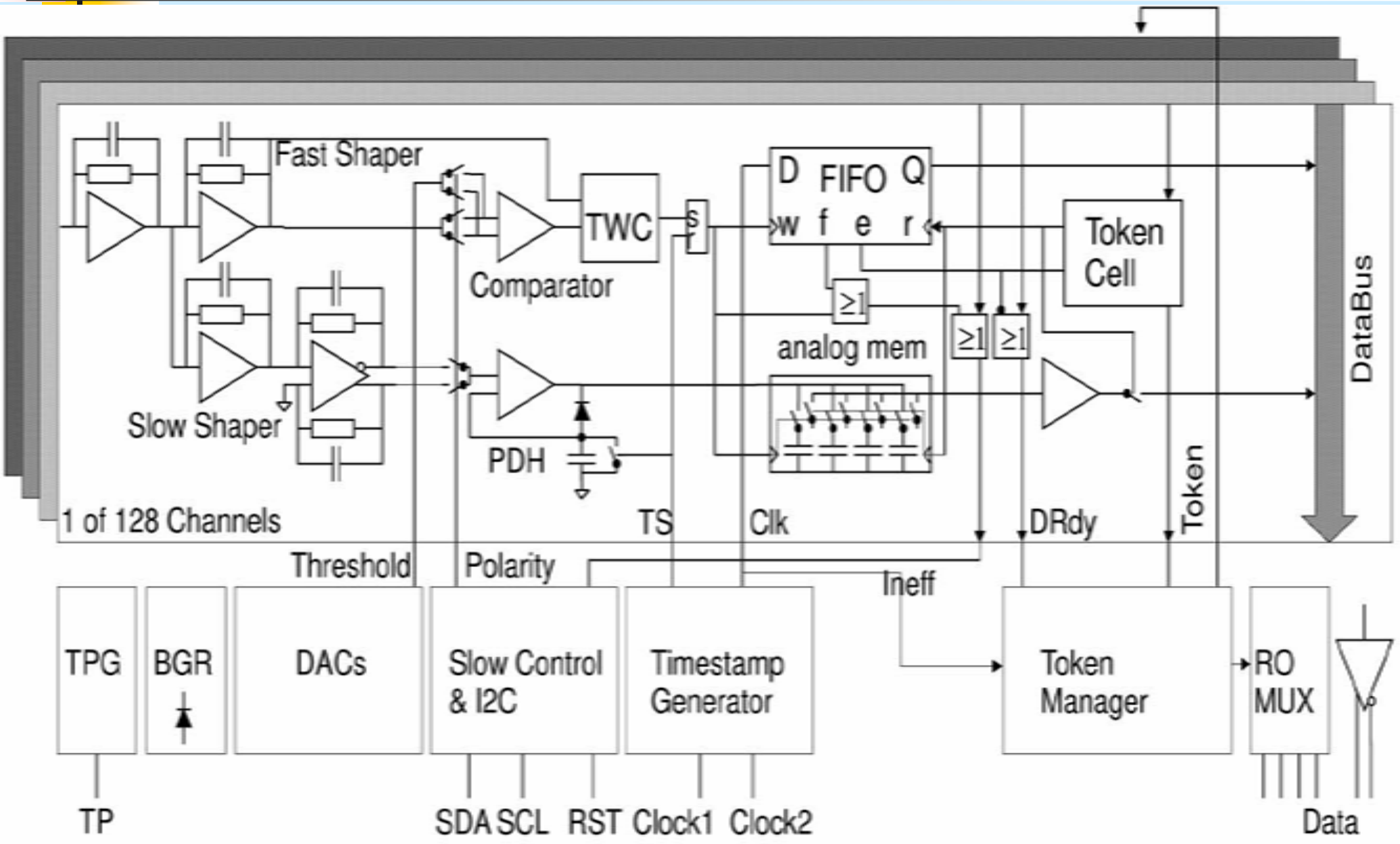
Front-End:

- 128 channel data driven charge sensitive front-end
- Front end for either polarity input signals
- Fast charge sensitive pre-amp and peak detector
- Time stamping with 1ns resolution
- Purely data driven, autonomous hit detection

Readout:

- Aanalogue energy and digital time stamp FIFO per channel (1ns resolution)
- De-randomizing, sparsifying Token Ring readout at 32 MHz

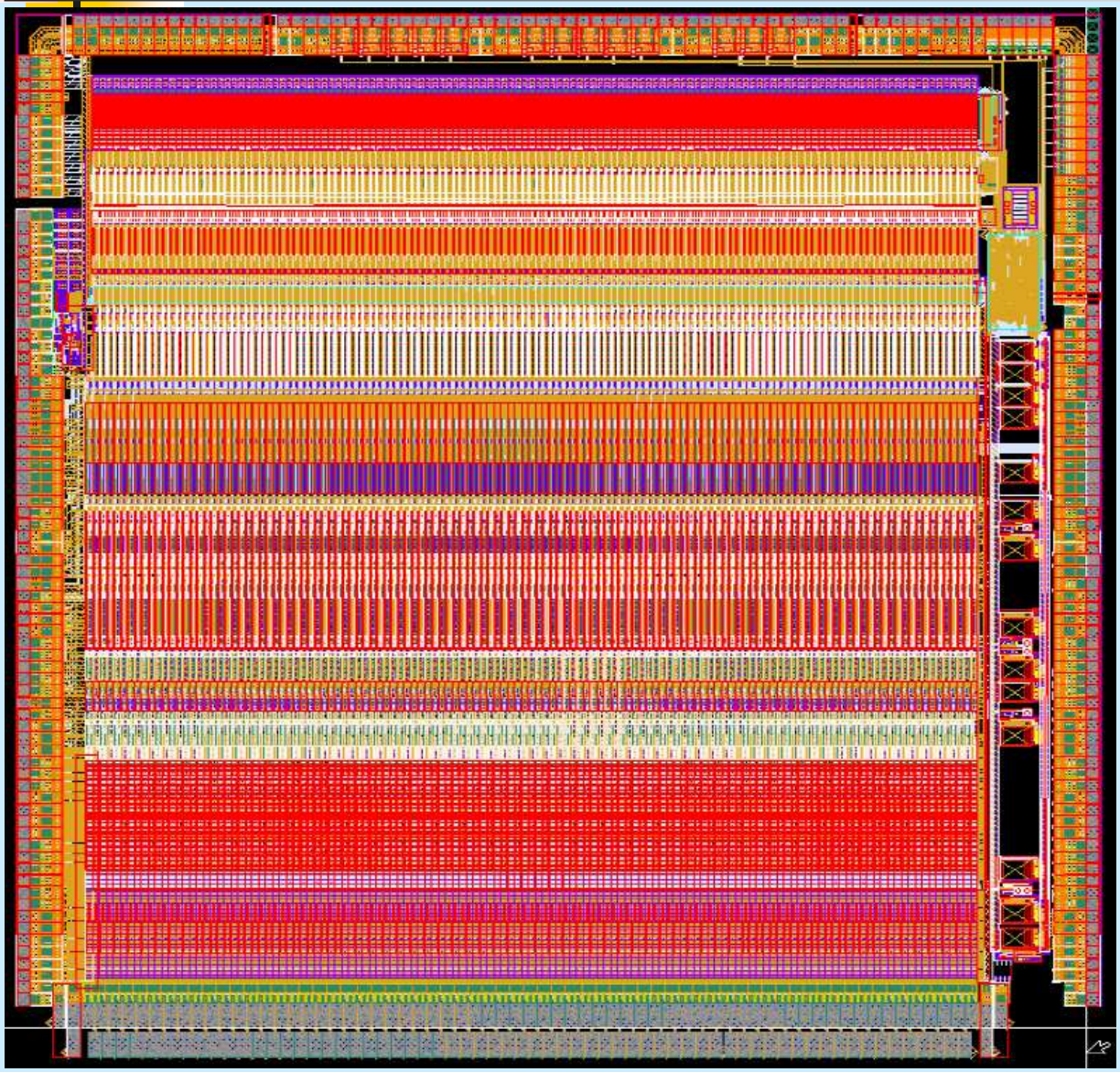
XYTER Architecture

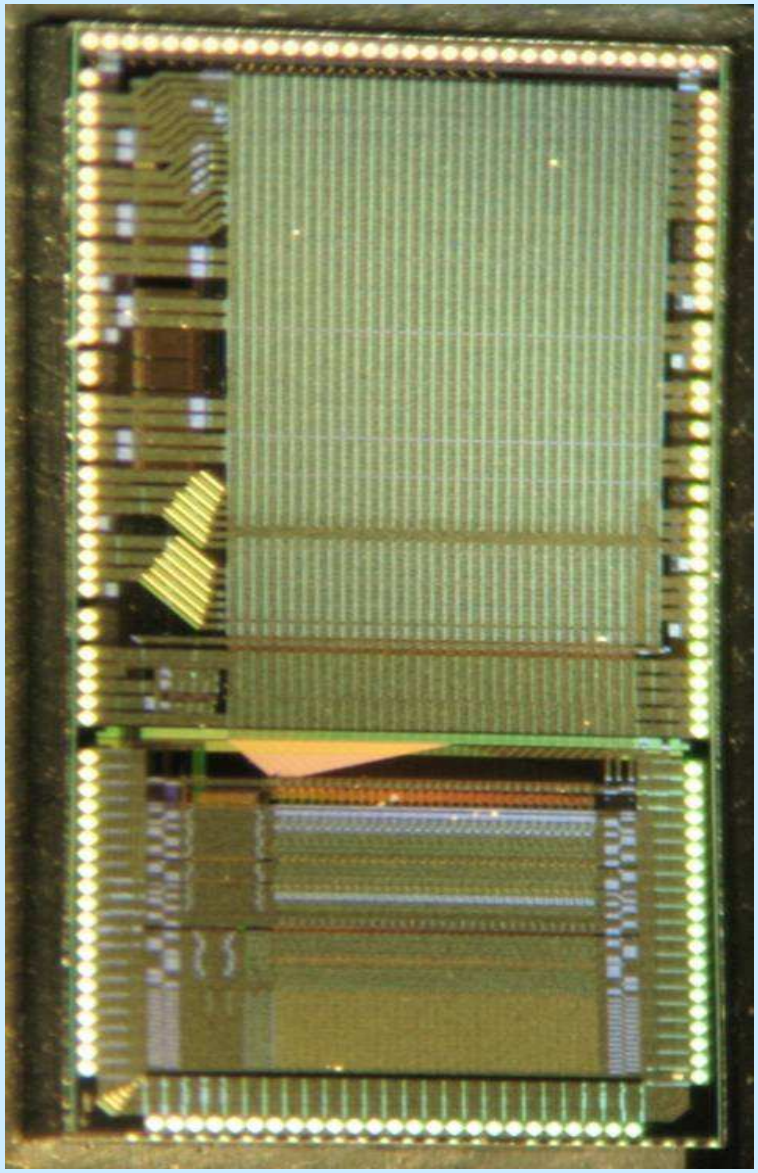


Slow Control: 8Bit Registers accessible by I^2C

- 16 mask registers with a mask bit for every channel
- 14 front-end adjustment registers for setting voltages and bias currents in the analogue part of the chip
- 2 configuration/status registers
- 2 diagnostic counters: token lost and FIFO-overflow
- 2 test-delay registers (useful for id. of pickup-paths etc.)
- 1 shift register 129 bytes deep for
  - local channel threshold trimming (bit 0 to 4) and
  - individual selectable analogue channel shutdown (bit 5)
- 3 delay registers for LSB time-stamp generation and tuning

AMS CMOS 0.35µ





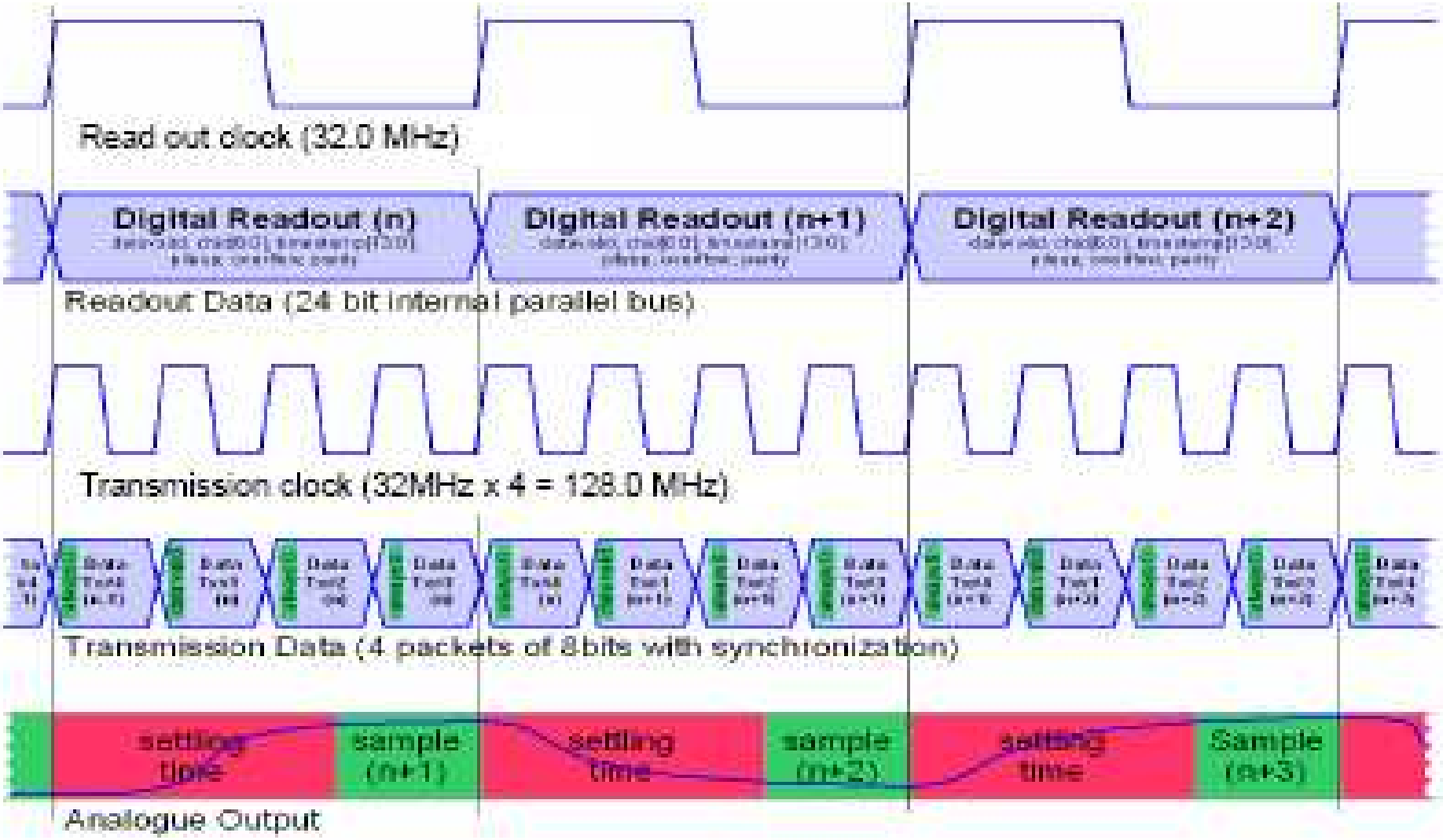
N_XYTER **MSGC_ROC**

Multiplexed ASICs 8-bit digital data output format

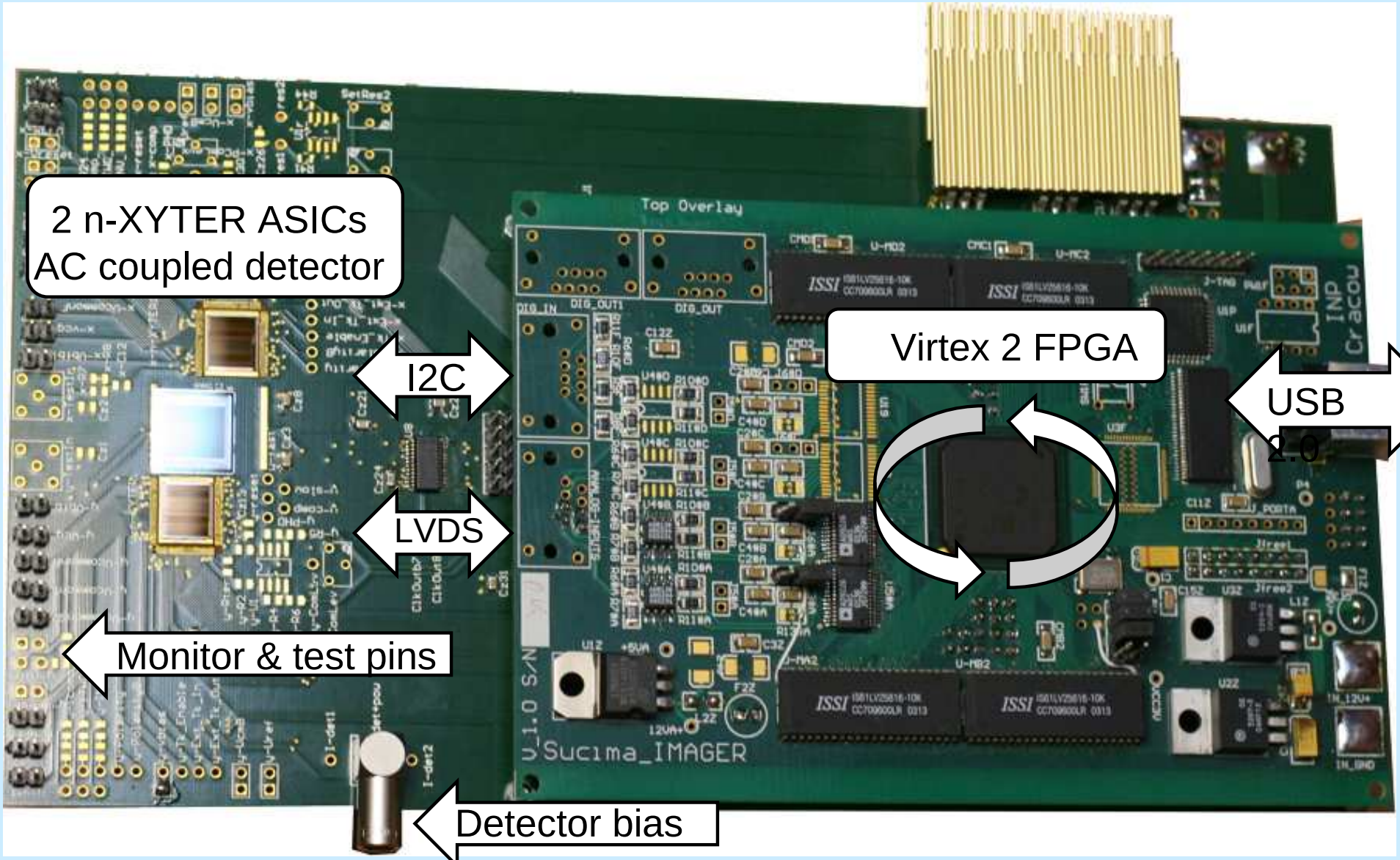
MSGC		Bits							
		7	6	5	4	3	2	1	0
Packets	0	DV1	0	0	TS11	TS10	TS9	TS8	TS7
	1	0	TS6	TS5	TS4	TS3	TS2	TS1	TS0
	2	0	0	0	(ID4)	ID3	ID2	ID1	ID0
	3	0	0	0	0	0	PileUp	OverF	Parity

Si-MSD GEM		Bits							
		7	6	5	4	3	2	1	0
Packets	0	DV1	TS13	TS12	TS11	TS10	TS9	TS8	TS7
	1	0	TS6	TS5	TS4	TS3	TS2	TS1	TS0
	2	0	ID6	ID5	ID4	ID3	ID2	ID1	ID0
	3	0	0	0	0	0	PileUp	OverF	Parity

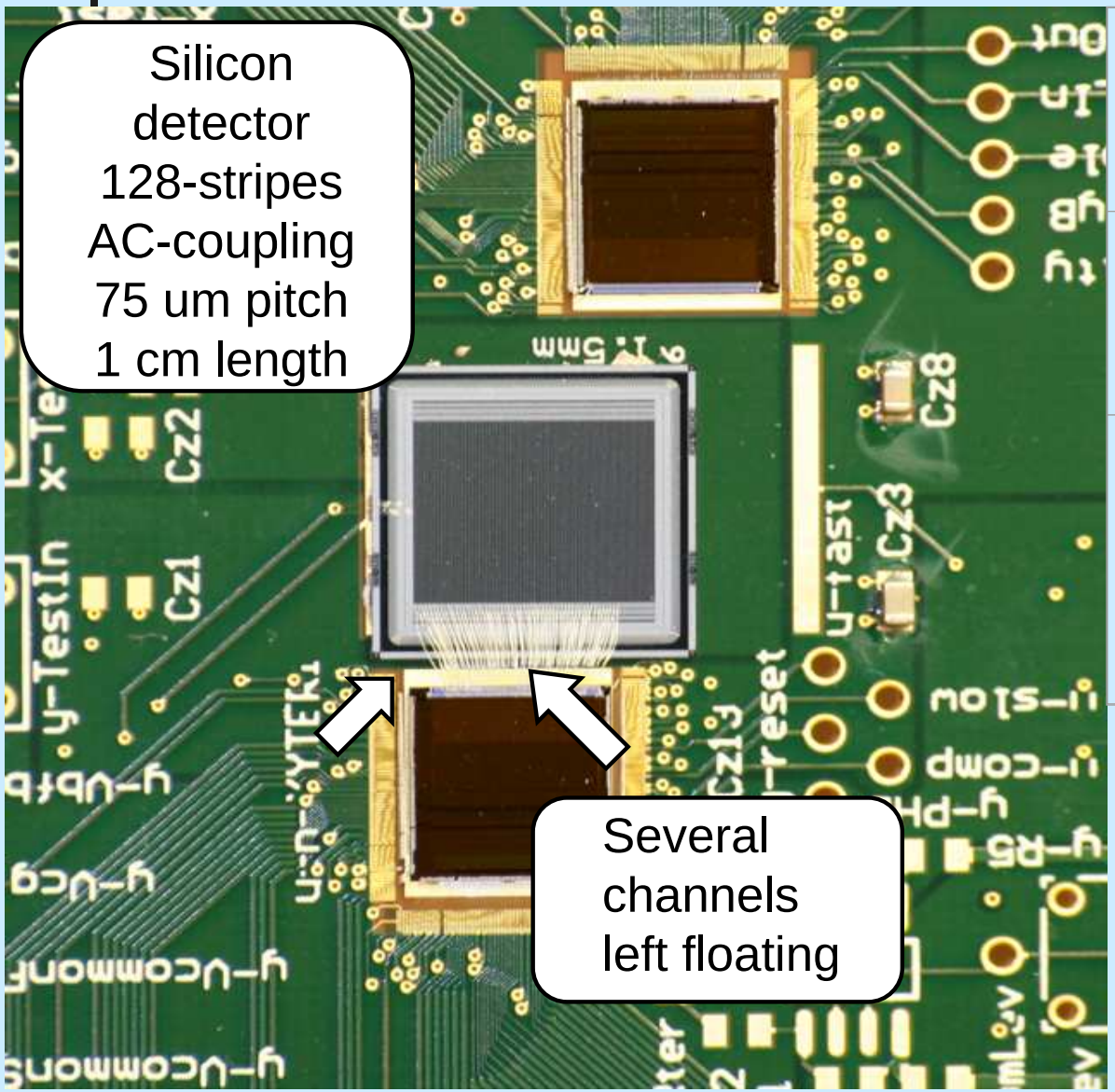
Timing diagram for multiplexed ASIC readout



n_XYTER TEST SETUP



Closer look

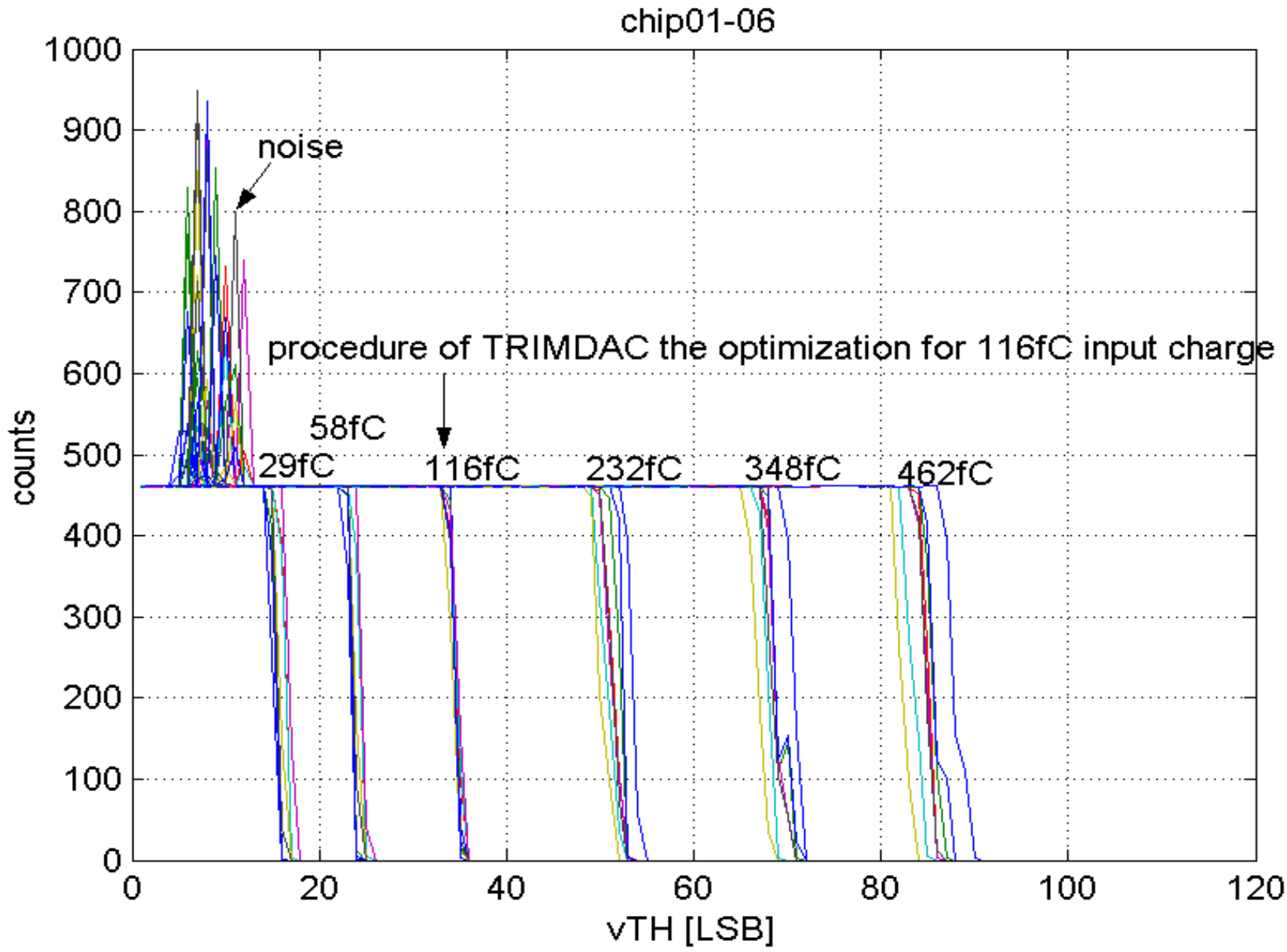


	FAST channel	SLOW channel
ENC	26.9 e/pF + 200 e	12.7 e/pF + 233 e
Peaking time	18.5 ns	139 ns

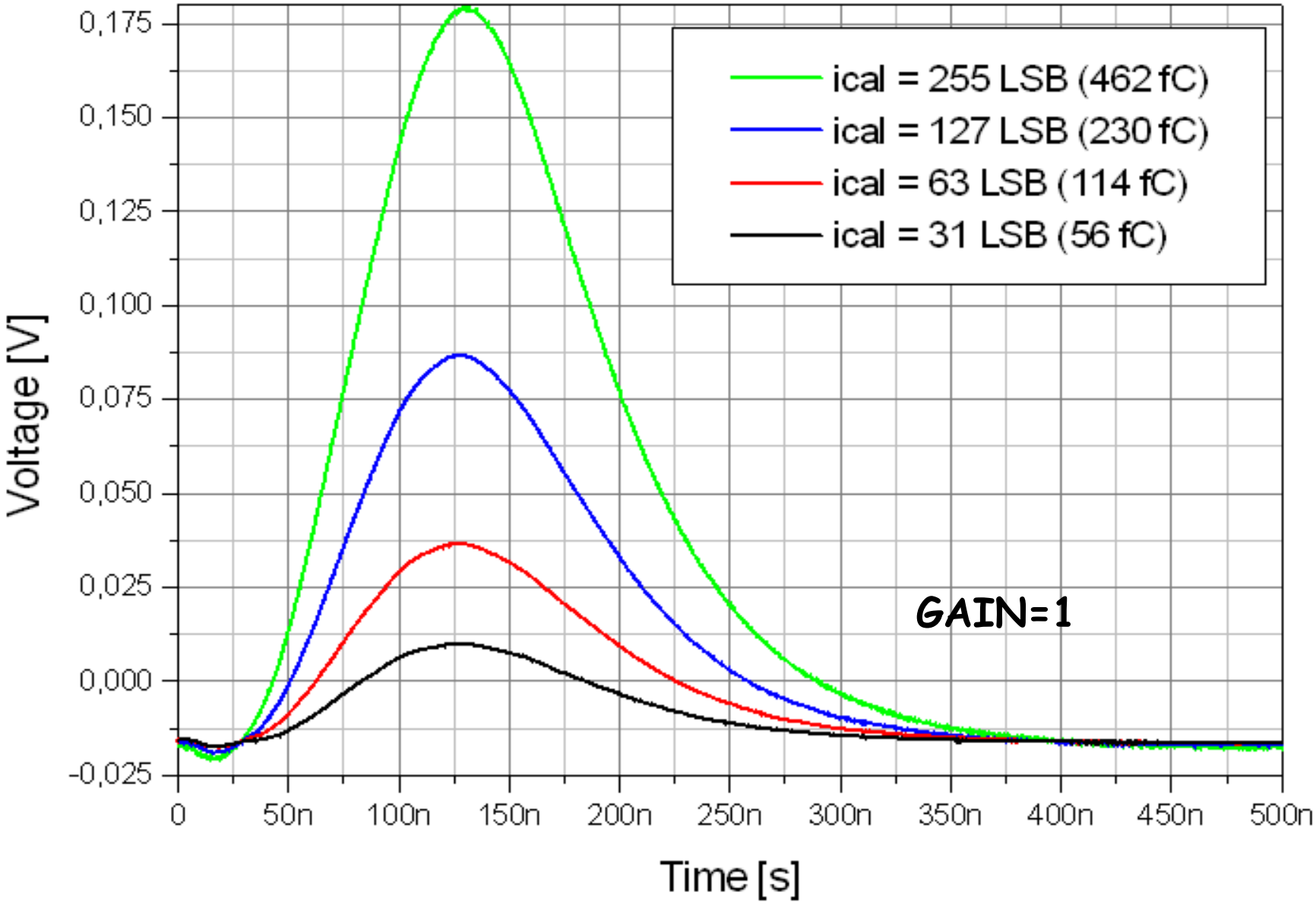
Engineered for 30 pF, giving
~1000 e ~600 e

pre-amp and shaper power consumption: 12.8 mW/channel

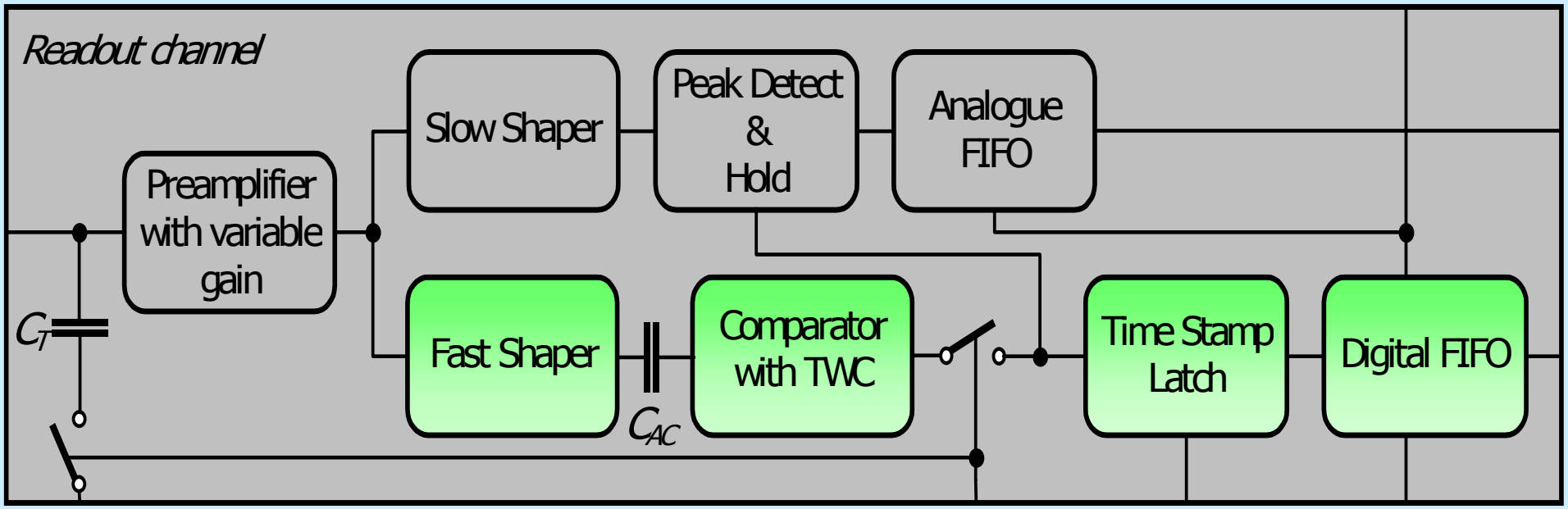
Trigger efficiency vs. threshold for different input charges after trimming the threshold



Pulse waveforms recorded at the output of slow shaper in the test channel for preamplifier

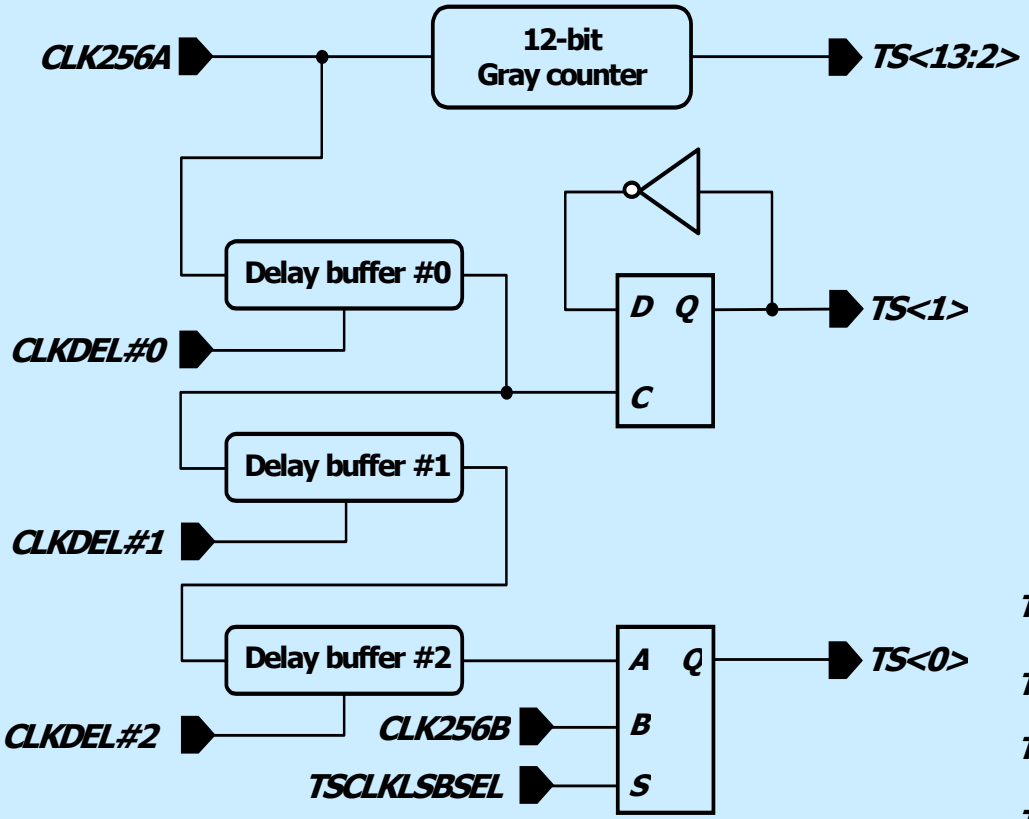


Timing channel



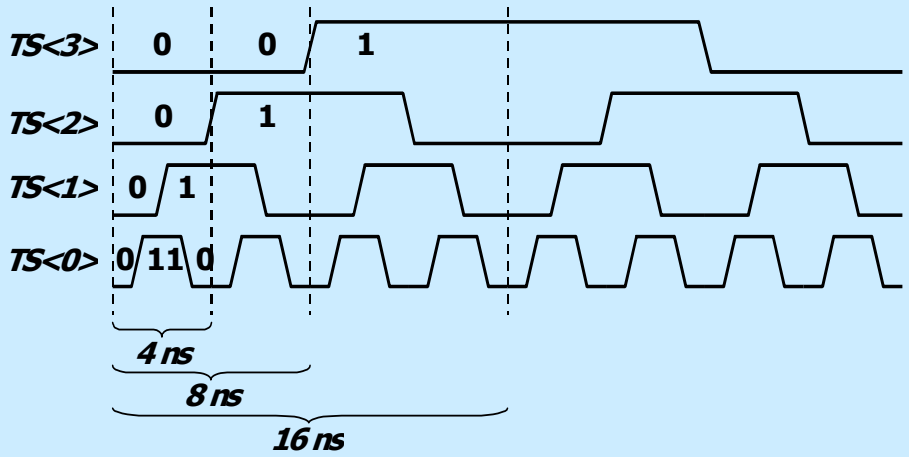
- Each comparator is equipped with a 5-bit trimming DAC, which allows to correct the threshold offset on the channel basis with a precision better than 1 LSB in the threshold DAC common for all channels

Time Stamp Generation



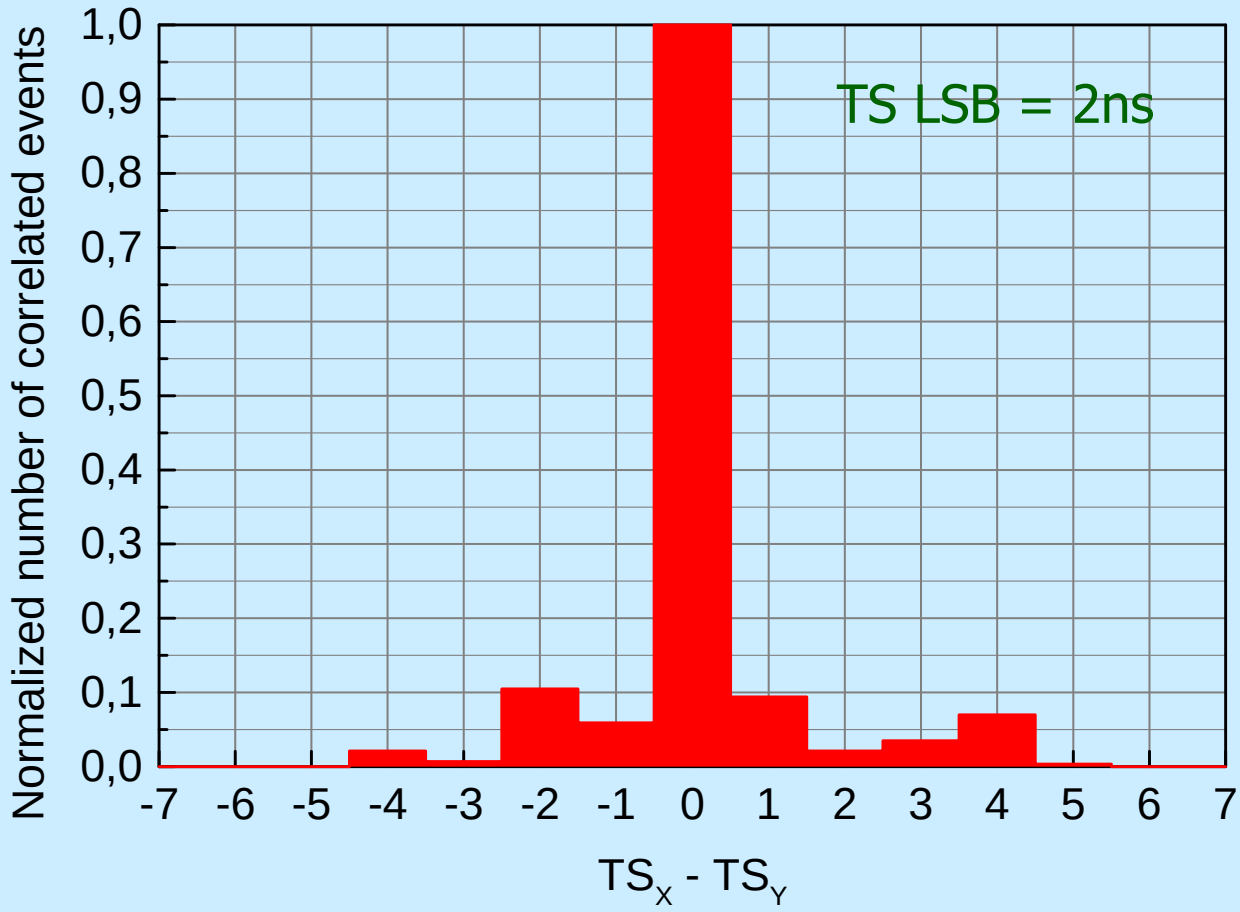
The 14-bit time stamp signature is combined of:

- 12-bit Gray-encoded counter,
- toggle flip-flop
- and input clock.



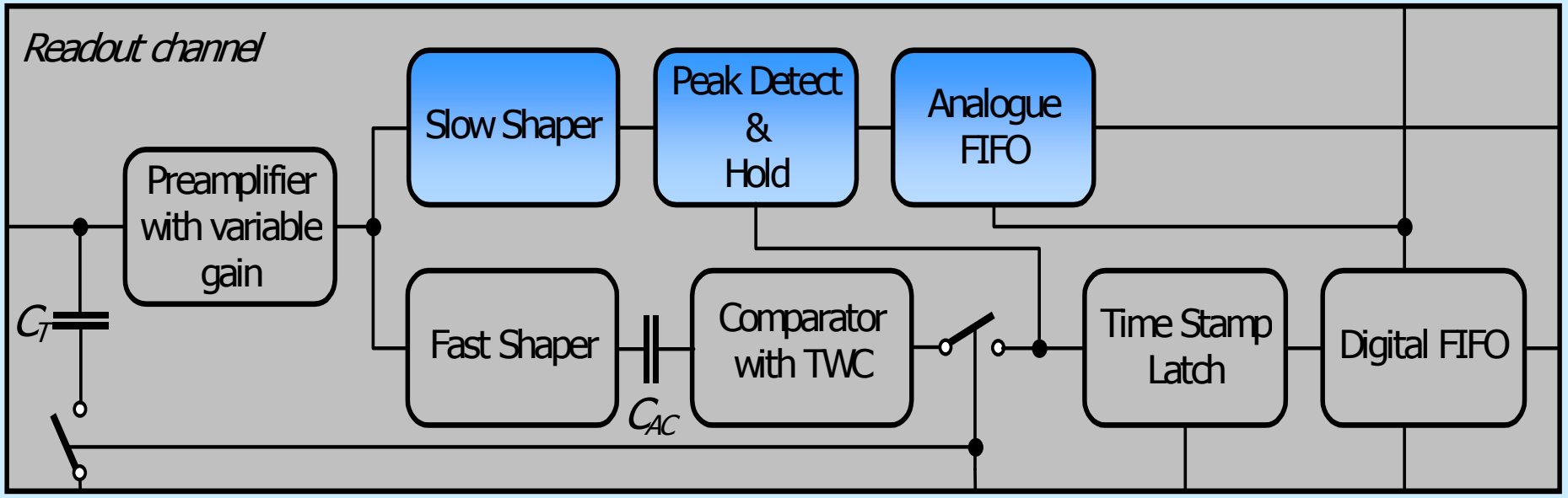
In this scheme we can achieve 1 ns resolution at 256 MHz input clock frequency.

Timing measurements



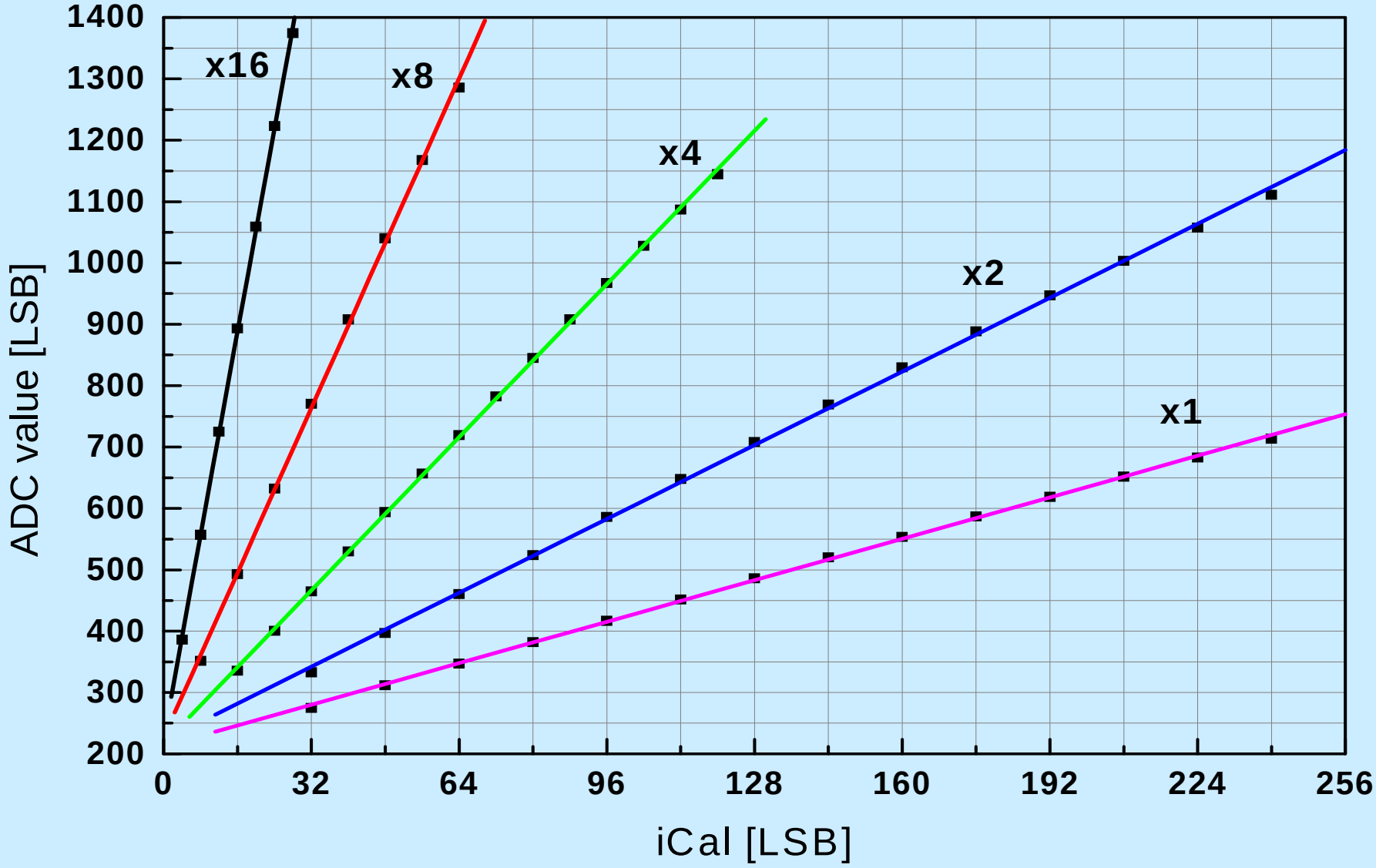
The histogram of Time Stamp coincidence between X and Y strips demonstrates the coincidence resolution of 2 ns as expected for the clock frequency of 128 MHz

Energy channel

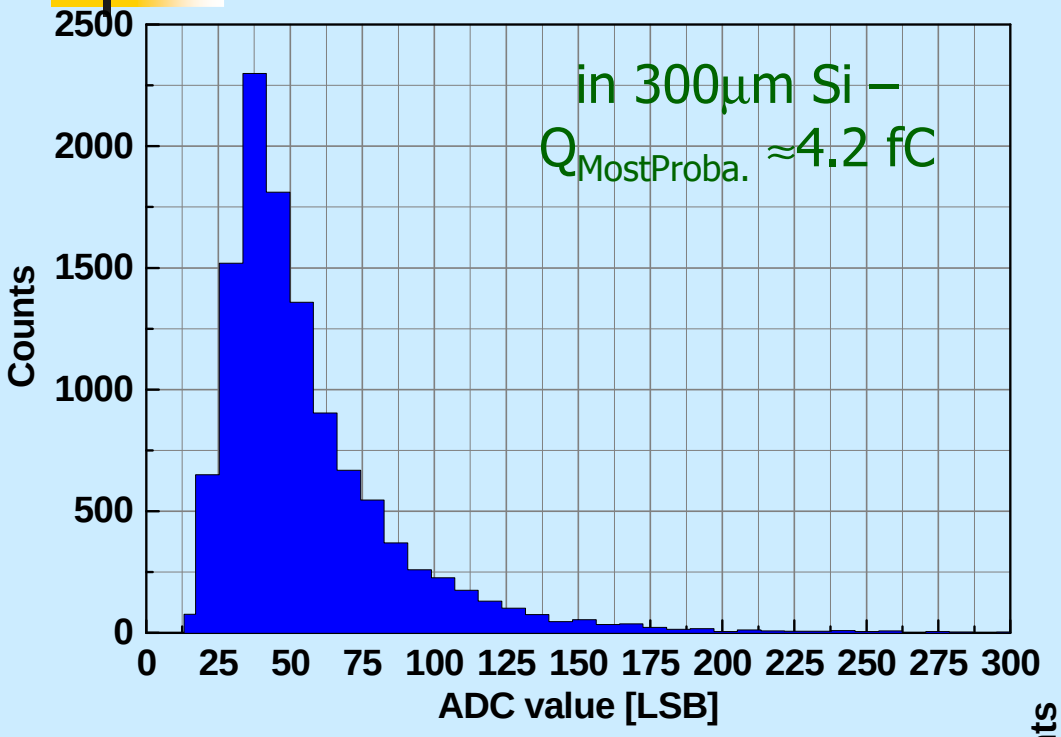


- The PDH circuit detects peaks of incoming pulses and holds their values for a given time period controlled with respect to the response of the comparator in the fast timing channel.

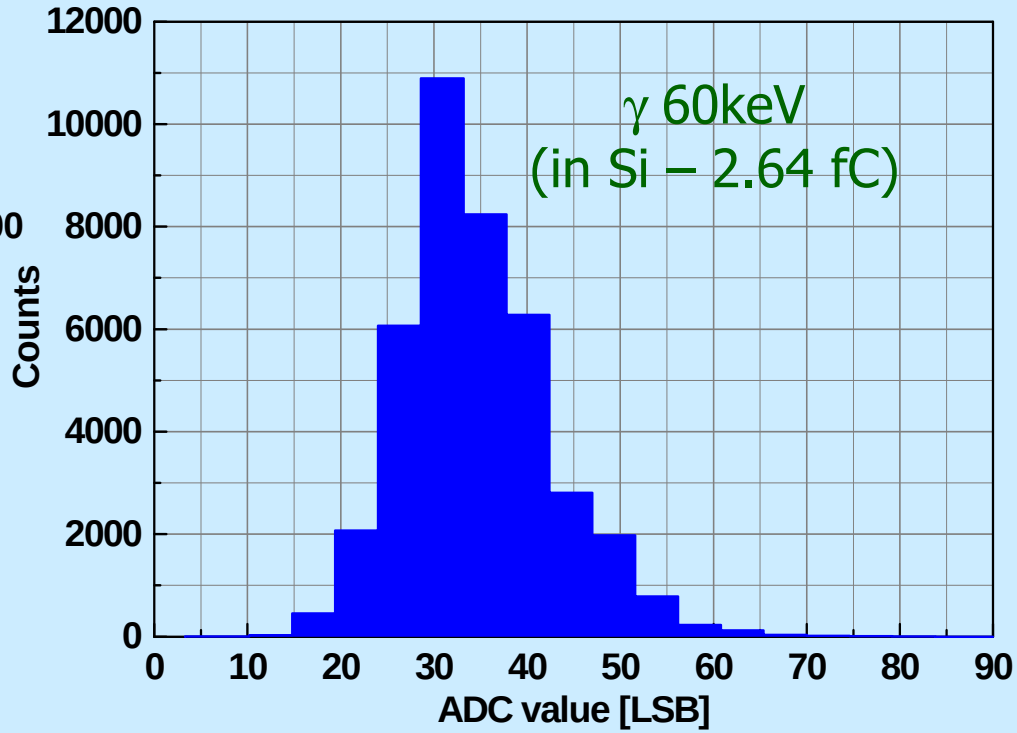
MSGCROC ASIC
Energy channel linearity



Energy measurements



Amplitude distribution
γ-rays ^{241}Am source
Gaussian distribution



Amplitude distribution
Electrons ^{90}Sr source
Landau distribution

Conclusions

- The tests performed on the *_XYTER ASICs demonstrate correct functionality of all building blocks.
- The analogue parameters, i.e. gain, noise and matching of parameters are in agreement with the design specifications.
- The critical digital circuits responsible for data derandomization and zero suppression token-based readout have been tested at a lower (128 MHz) clock frequency compared to the nominal one (256 MHz).
- There are, however clear indications that the ASIC should work correctly at higher clock frequencies.
- In the near future tests of two chips connected to DS_Si strip detector will be performed.

CBM-XYTER Architectural Specifications

	CBM STS	CBM MuCh	PANDA STS	PANDA TPC
charge pol.	+/-	+ or -	+/-	-
no channels	128	128	128	128
sparsification	yes	yes	yes	yes
self trigger	yes	yes	yes	yes
differential i/o	yes	yes	yes	yes
rate per channel	250 kHz	200 kHz	75 kHz	200 kHz
time stamp	yes	yes	yes, 2 to 20 ns	yes, 5 ns
double hit res	100 ns	100 ns		200 ns
energy r/o	yes, 8bit	yes	yes, 10 bit	8 bit
ch fifo depth	16	16		
rad. level	1 MRad	1 MRad	1 MRad	0.1 CMS STS
ch pitch	50 µm	100 – 200 µm	50 µm	100 – 200 µm
DC-bias, leakage	no	no	yes ?	no
power	high concern	no concern	3 mW	less concern
no of chips			5000	1000

Front End Relevant Specifications

	CBM STS	CBM MuCh	PANDA STS	PANDA TPC
charge pol.	+/-	+ or -	+/-	-
energy r/o	yes, 8bit	yes,	yes, 10 bit	8 bit
ENC	1000 – 2000	2000	1000 – 2000	2000
dynamic range	MIP (23 000 e^- ?)	MIP	160 000 e^- (7 MIPs)	200 000 e^-
power	high concern	no concern	3 mW	less concern
S/N (MIP)	> 12		> 12	
inp. pulse dur.	10 - 25 ns	10 – 30 ns	10 – 25 ns	
input cap.	50 pF	15 pF	30 pF	10 pF
rate per ch	250 kHz		75 kHz	200 kHz
double hit res.	100 ns	100 ns		200 ns
rad. level	1 MRad	1 MRad	1 MRad	0.1 CMS SiTr

Specifications at this point are usually a mooving target. Consider this collection as a starting point for further iterations...

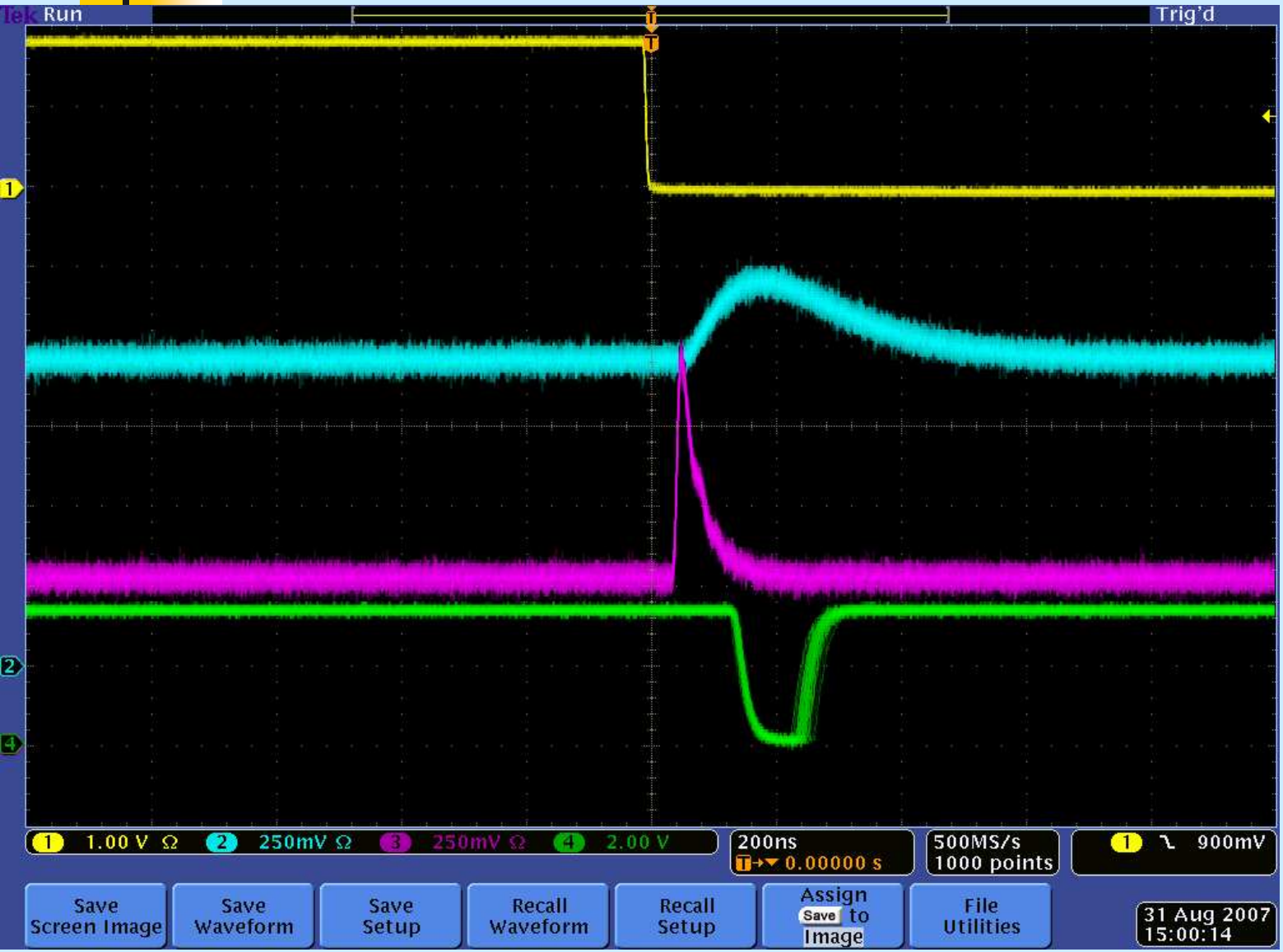
CBM_STS Targeted Specifications

- 800 ENC on the timing channel
- 30 pF detector capacitance
- 500 kHz per channel, 5% occupancy
- DC coupling, leakage current compensation
- Channel pitch 40 µm, detector strip pitch 60 µm
- Maximum design size 5mm x 5mm
- 2,6 Gbit serial interface for data transfer
- Data element 32bit
- Energy resolution ? 7 to 10 bit?
- ADC for each channel ?
- Technology UMC 0.180 µm ?

END

- Thank you for the attention

Analogue Signal Sequence (Test Channel)



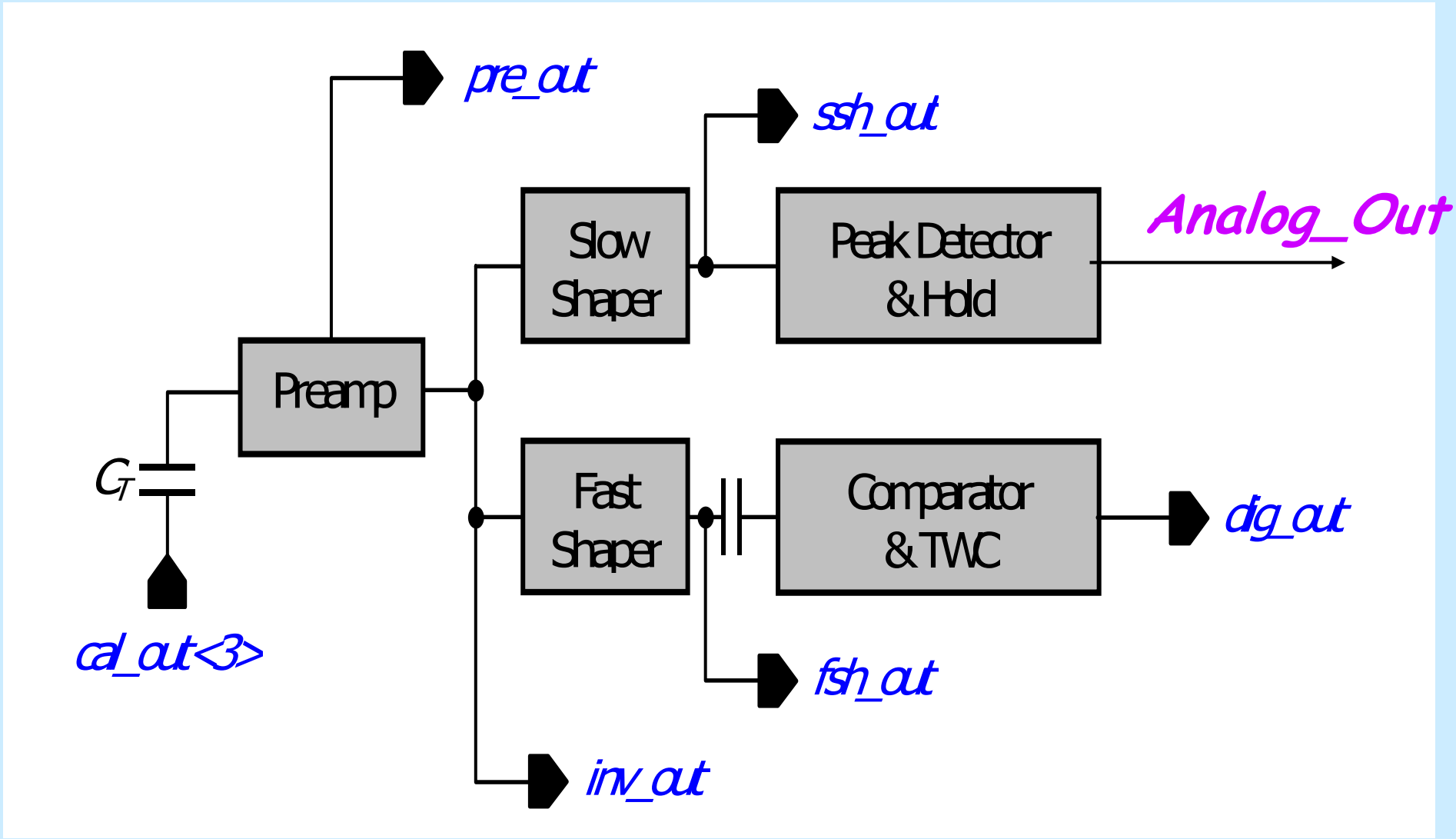
Test pulse Release

Slow Shaper

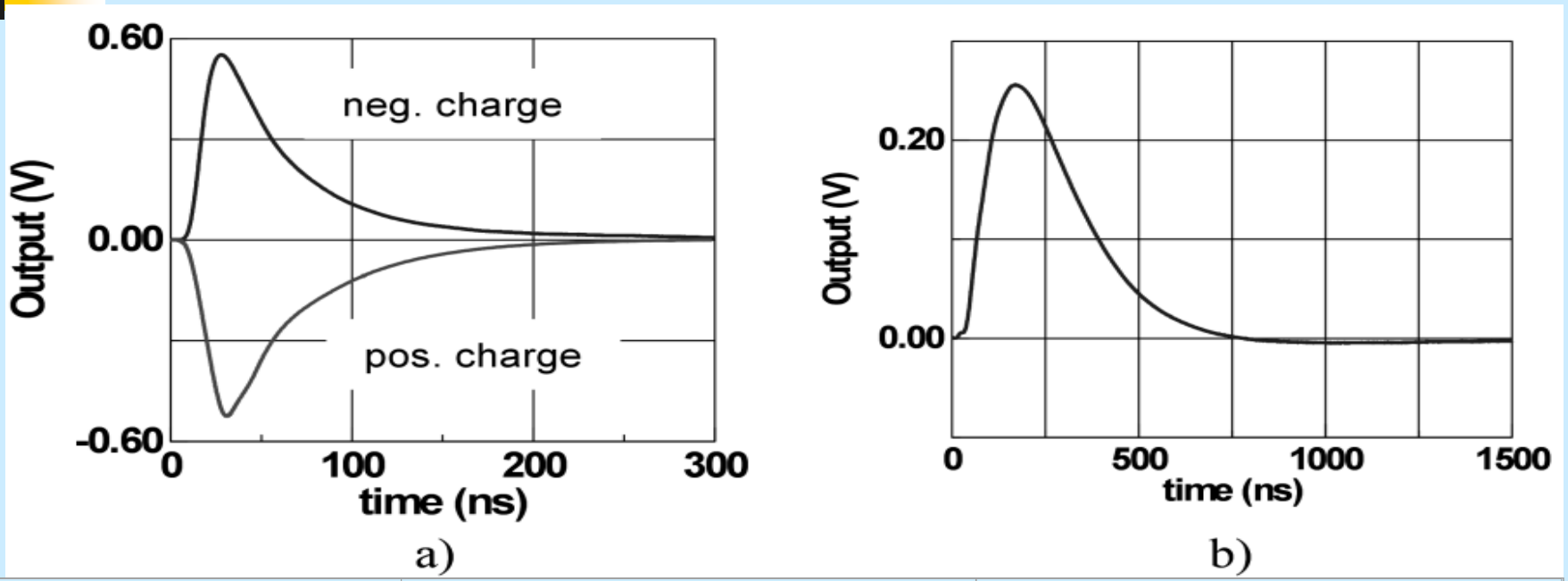
Fast Shaper

Discriminator Output

Block diagram of the test channel and locations of the test pads



Analogue Pulses, Peaking Time, Front-End Noise

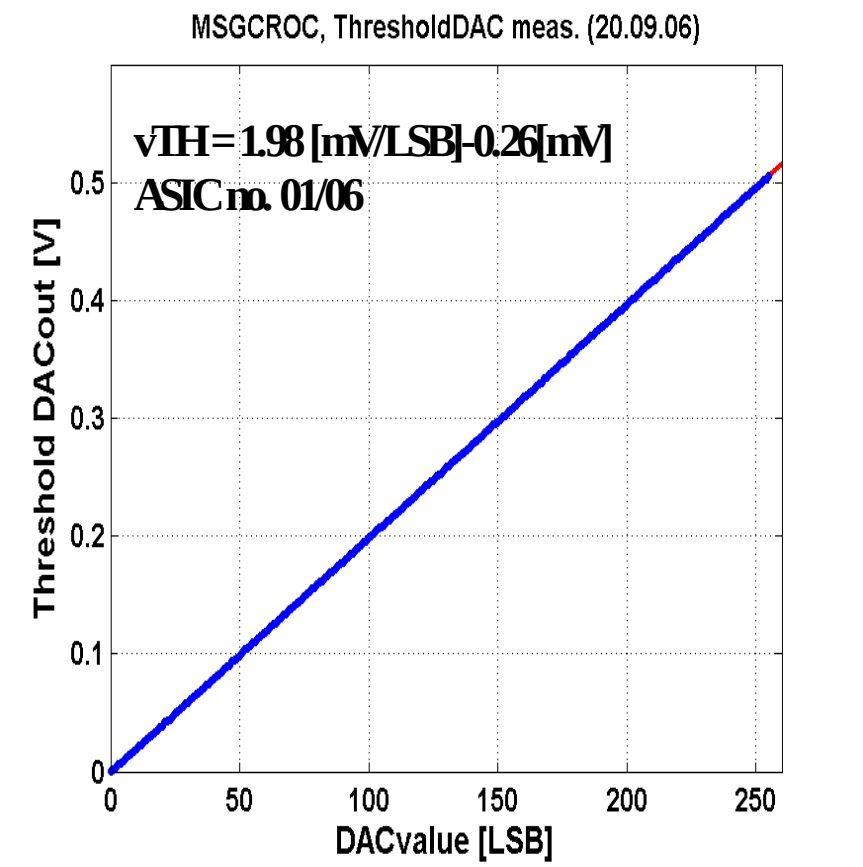


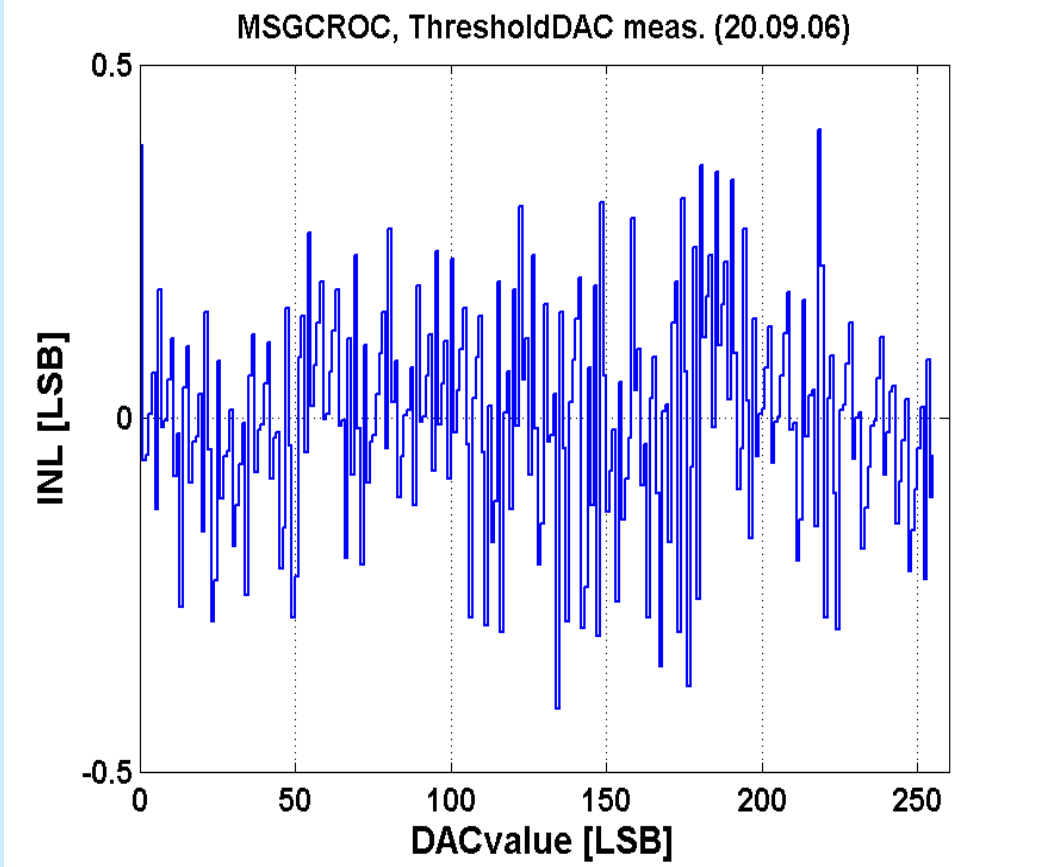
	FAST channel	SLOW channel
ENC	26.9 e/pF + 200 e	12.7 e/pF + 233 e
peaking time[a] (1% to 99%)	18.5 ns	139 ns

Engineered for 30 pF, giving (850) 1000 e 600 e

pre-amp and shaper power consumption: 12.8 mW per channel

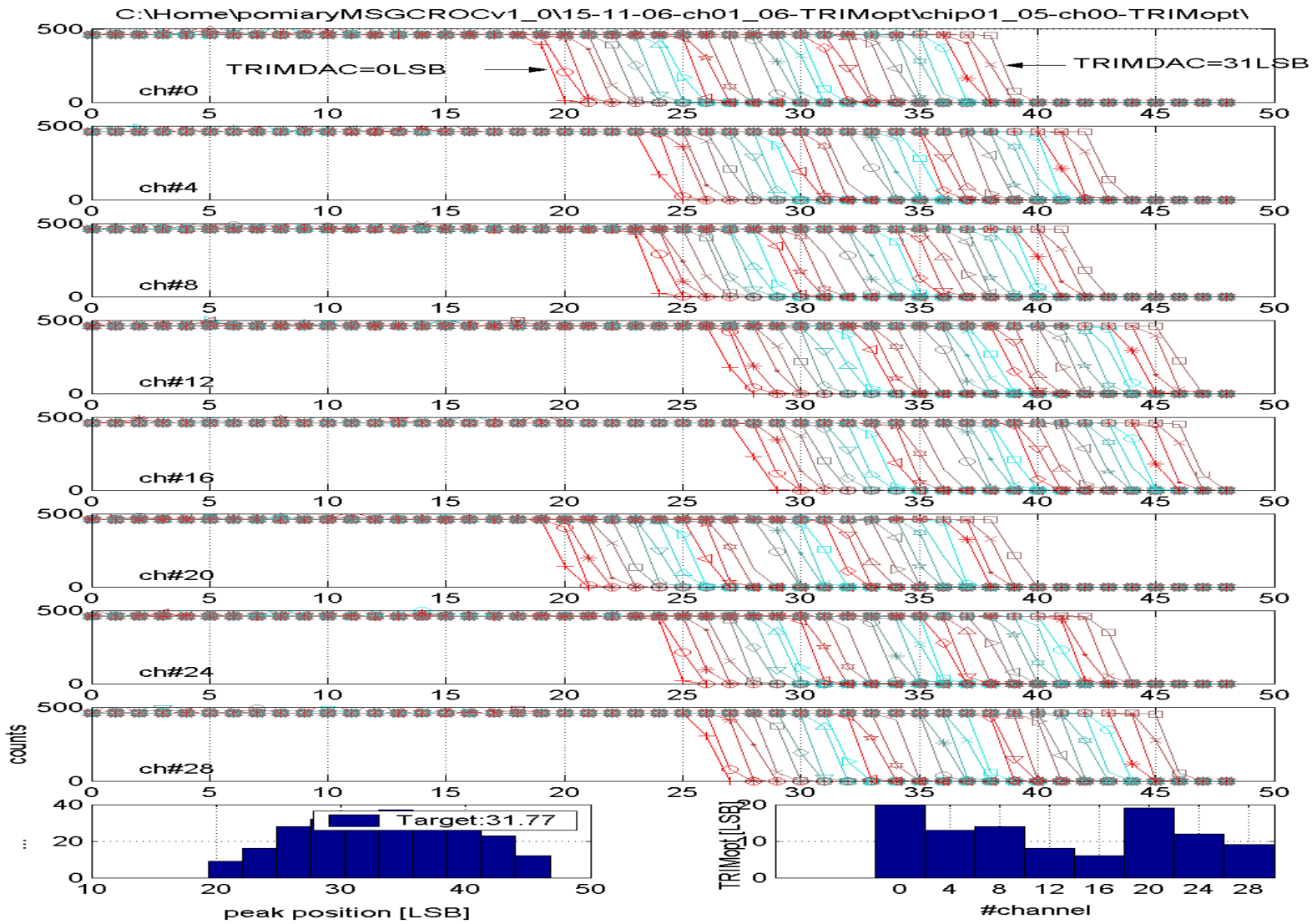
Response curve and integral nonlinearity of the threshold DAC





Till now 8 ASICs have been tested

Trigger efficiency vs. threshold for channels: 0, 4, 8, 12, 16, 20, 24, 28



Threshold offset correction TrimDACs values (6-24)