

Time Stamping Task- Introduction and Work Group Overview

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Overview of talk:

- ***Introduction:***
 - *What is Time Stamping?*
 - *Why do we do it?*
 - *How do we do it?*
 - *Problems to consider.*
 - *Examples of Time Stamping*
- ***Working Group***
 - *What should we do?*
 - *Who will participate?*

What is Time Stamping?

- *Associate time label with data from a channel, a sub-system or a system.*
- *Fixed time relationship to moment when channel fired or event generated*
- *Permits the use of these time stamps to correlate data within detectors, between detectors, between systems.*
- *Simplest form is to correlate multiple free running systems (c.f. 1991 RDT experiments at Daresbury NSF)*
- *Note: Hardware triggers can be used too if necessary but many benefits of TS are lost if data is thrown away in this way.*

Why do we do Time Stamping?

- *Eliminates dead time (but not pileup)*
- *Allows software triggering which hugely increases flexibility:*
 - *Software can look back/forward in time (time=buffer size)*
 - *Can take 100% of low rate in delayed coincidence with high rate (minimal dead time losses)*
 - *Can correlate multiple systems without cross-triggering cables.*
 - *Can easily do multiplicity triggers in systems with huge channel counts*
 - *Eliminate huge number of trigger connections (no problems from cables, ground/isolation)*
 - *Overcome latency in pipelined processing (digital or analogue)*
- *Summary: Better data selection*

How do we do Time Stamping?

- Need stable clock, lined up everywhere (adjust delay/phase)*
- Need local TS logic in channel/sub-system/system*
- Need a regular pulse to “timeframe” data (and lack of data)*
- Need a powerful processing system and lots of memory*
- Can be used with analogue or digital signal processing.*
- Can be used alongside conventional hardware triggered readout, but with limited results.*

Problems to consider when Time Stamping?

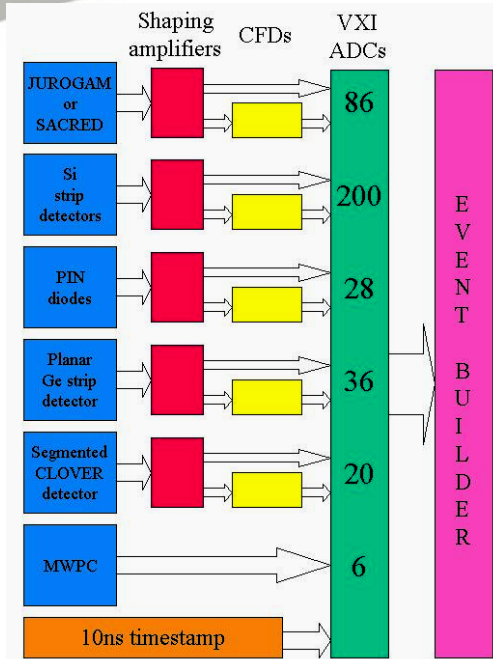
- *Need timestamps in ASICs (c.f. XYTER talk, also STFC CZT ASIC, CALICE MAPS, planned R3B Si ASIC. Others?)*
- *Latency- doesn't matter until we make connections to ancillary detectors- cross-system triggers with analogue triggers*
- *Buffer edge effects (time/channels)*
- *Time alignment (setup) is critical*
 - *sub ns for AGATA PSA*
 - *for simple coincidence must be better than half a clock across all systems*
 - *for ToF must be few tens of ps (or calibrated)*
- *ToF not easy- TS is only as accurate as the clock (or clock divided by 2 or 4) after alignment and jitter errors.*
 - *For ps ToF timing we still need to use TACs*
 - *Should also calibrate the ToF channels for clock alignment errors*
- *Bandwidth for readout of high rate beam tracking (or links to feed in lists of interesting timestamp ranges to local readout)*



Examples of NP Time Stamping Systems

- *GREAT TDR (UK/Finland, Jyvaskala)- working*
- *CENTRUM (GANIL)- working*
- *CENTRUM plus ATOM (GANIL) under design?*
- *AGATA GTS system (Europe) designed; being built*
- *BUTIS (GSI/FAIR) Built (local distribution being specified)*

Time Stamping example 1 - GREAT TDR



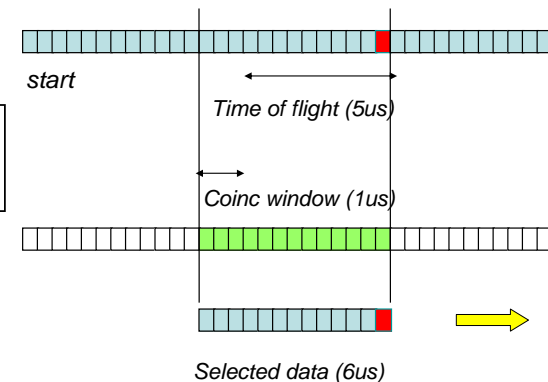
Rack includes

- 4 NIM and 2 CAMAC for front end Amps, CFDs.
- A VME crate (data merger, metronome and pattern unit)
- 2 VXI crates containing between 12 and 15 32 channel cards (up to 480 channels).

GREAT data selection

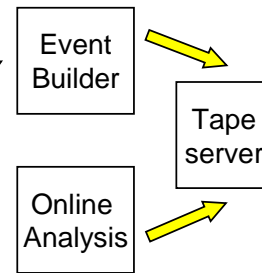
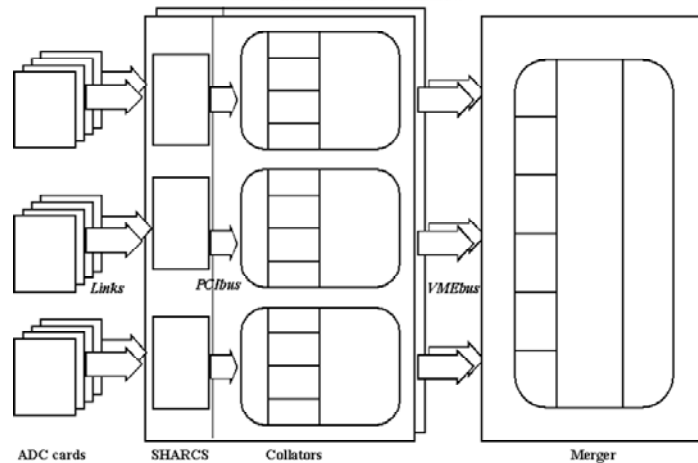
- Recoil data from focal plane
- Ge data from target array
- Time window

Time-ordered input data stream

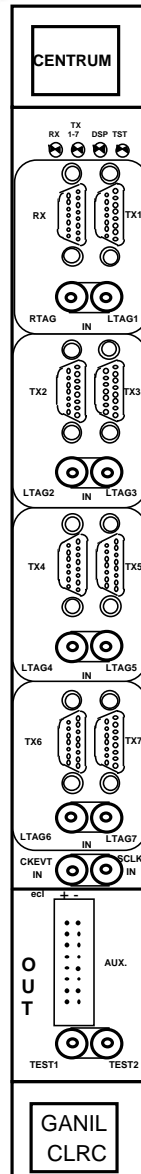


TDR software data flow

Single stream of time ordered data to event builder.



Time Stamping example 2 - CENTRUM



VXI-C

- Time Stamps Events (not channels)

- Correlates EXOGAM with VAMOS and TIARA

- ATOM upgrade adds channel timestamps

Time Stamping example 3 - AGATA

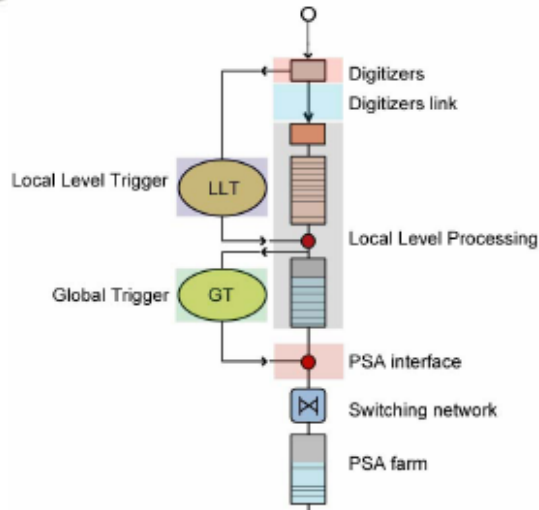


Fig. 1. The AGATA readout column.

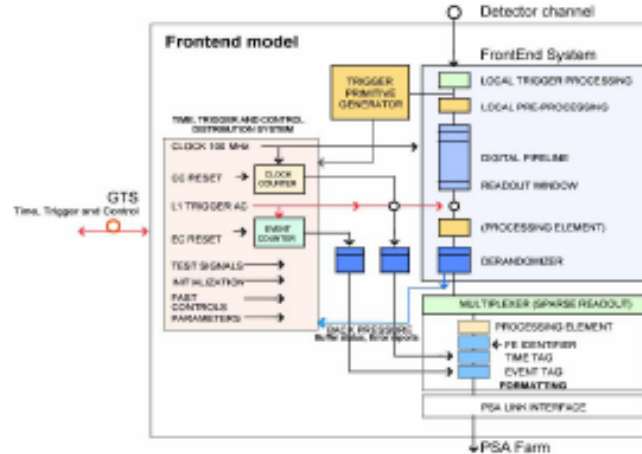
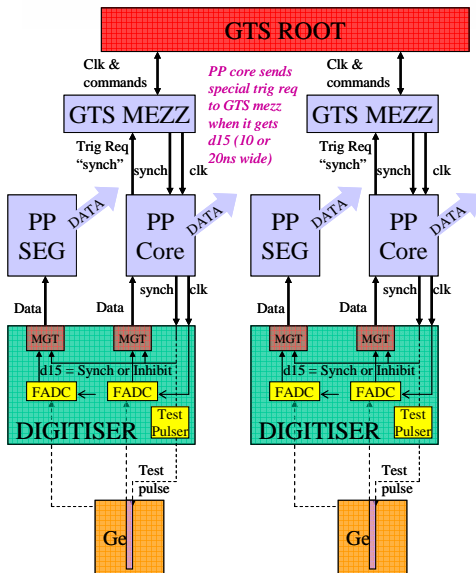
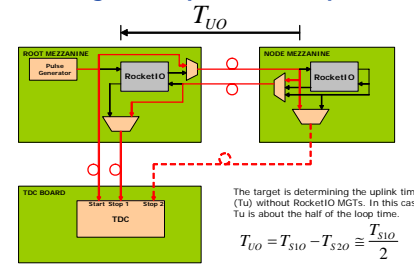


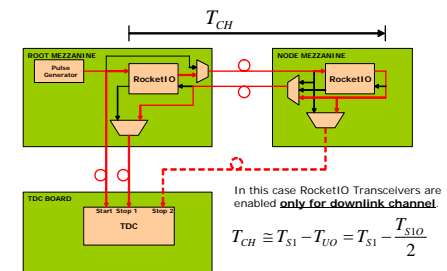
Fig. 2. Model of a detector channel.



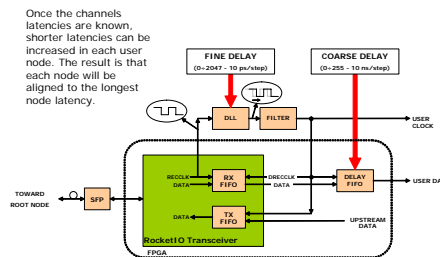
Alignment process: step 1



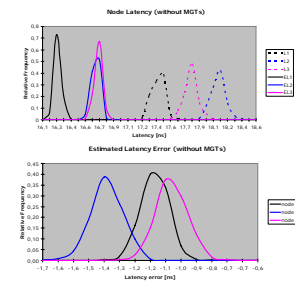
Alignment process: step 2



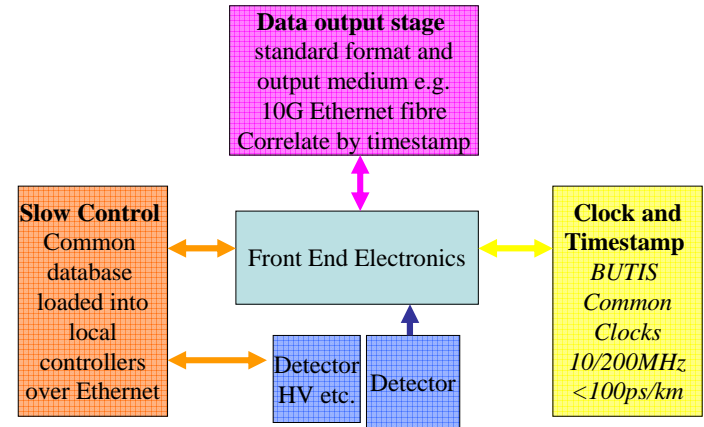
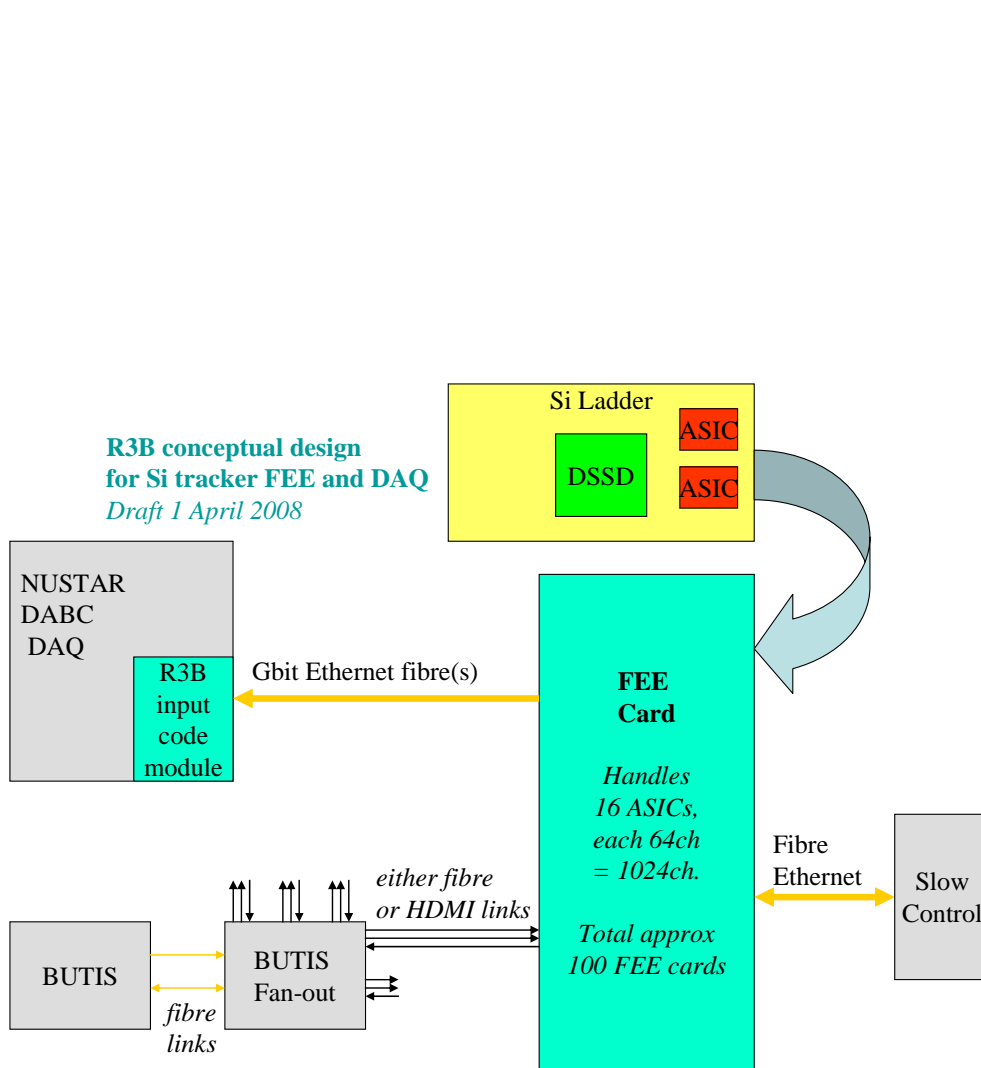
Alignment process: step 3



Systematic Errors



Time Stamping example 4 - NUSTAR (BUTIS)

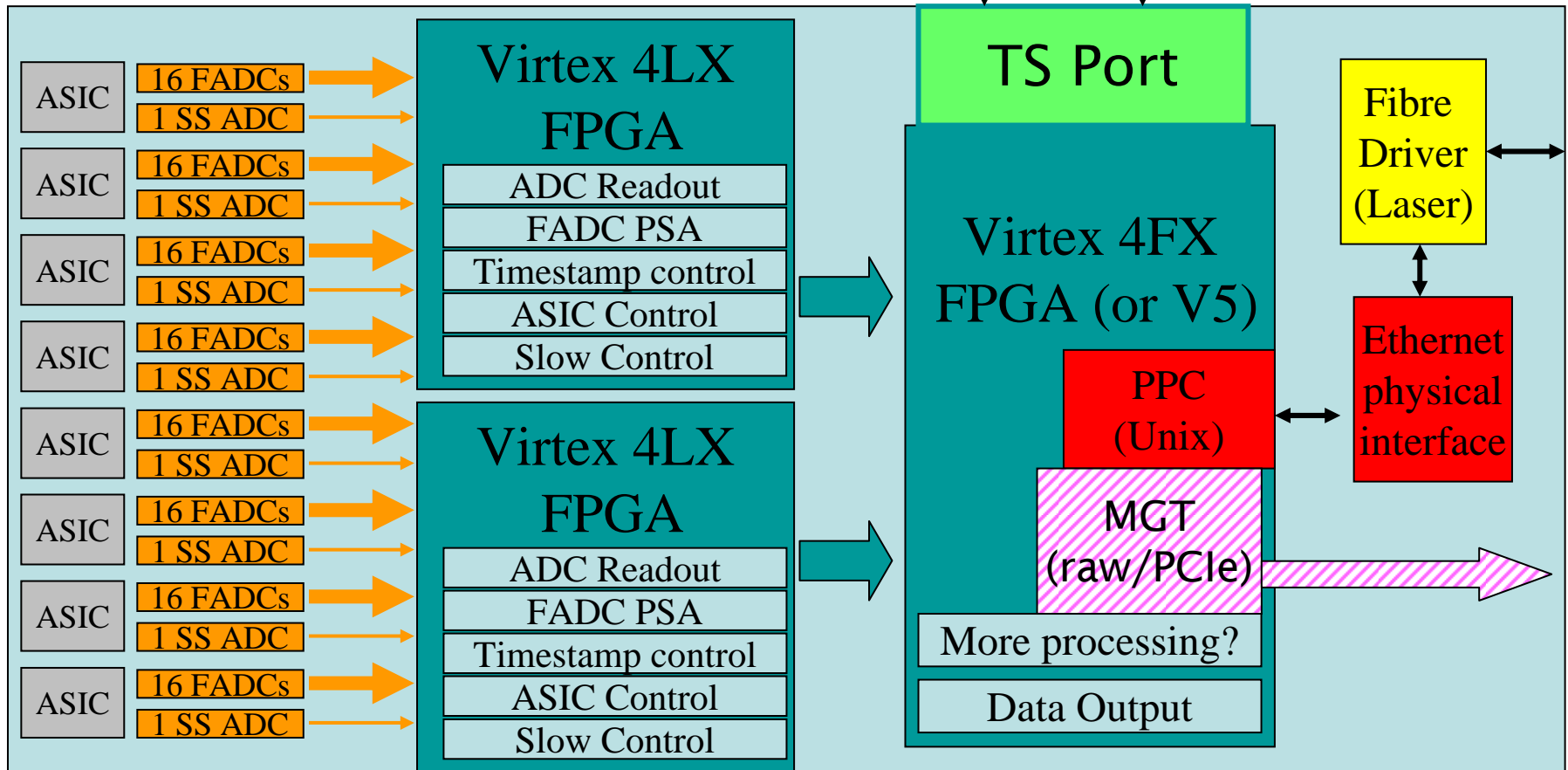


More later from Haik...

Time Stamping example 5 - AIDA (DeSpec)

16 ch
ASIC

16 FADCs (12/14 bit)
1 Sliding Scale ADC
(14bit) per ASIC



Time Stamping Working Group

- *What shall we do?*
 - *Review existing systems*
 - *Review planned systems*
 - *Exchange information*
 - *Consider strengths and weaknesses of known systems*
 - *Should we standardise on one system?*
 - *Can we make a common TS port (c.f. AIDA for DeSpec)*
- *Who will participate?*
 - *All are welcome...*