



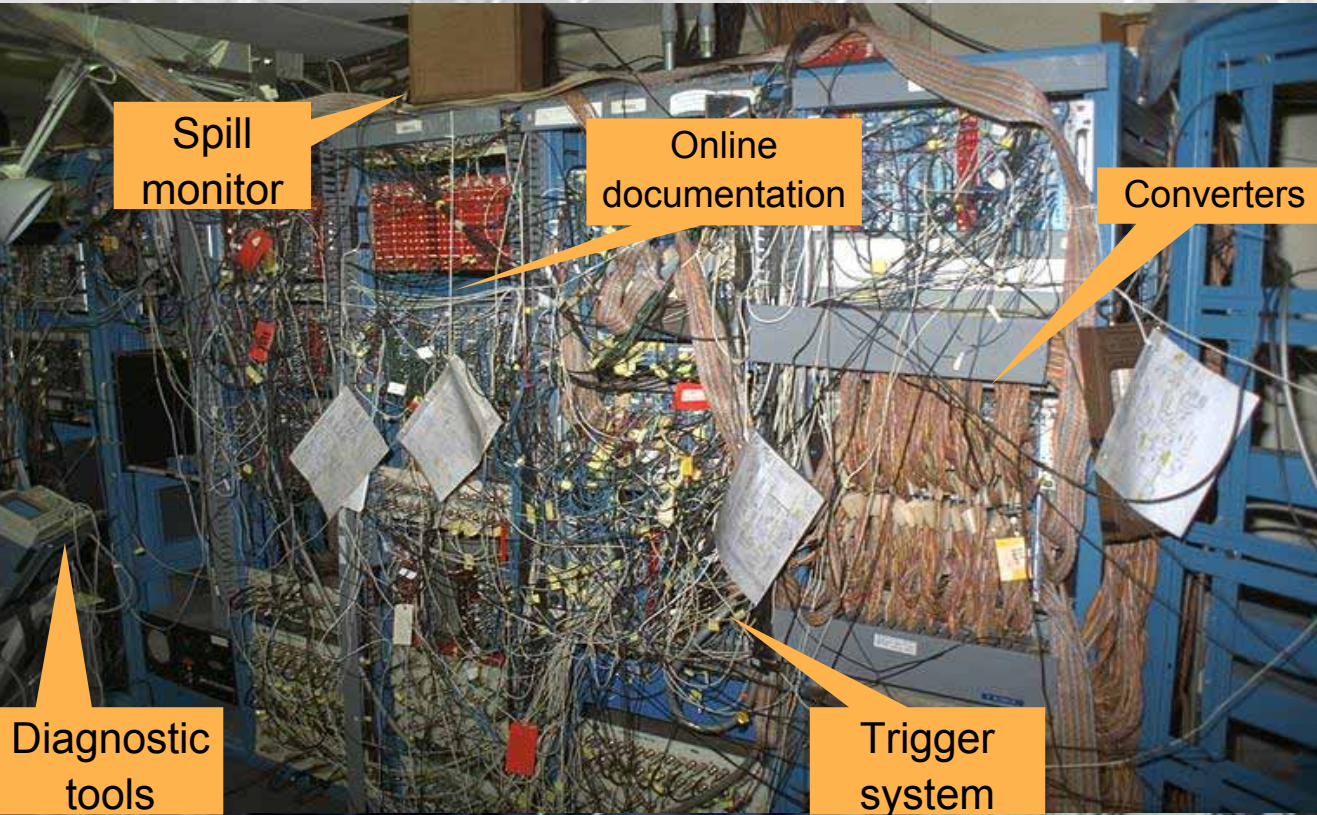
# Off go the ...

**H. Simon – GSI-Darmstadt**

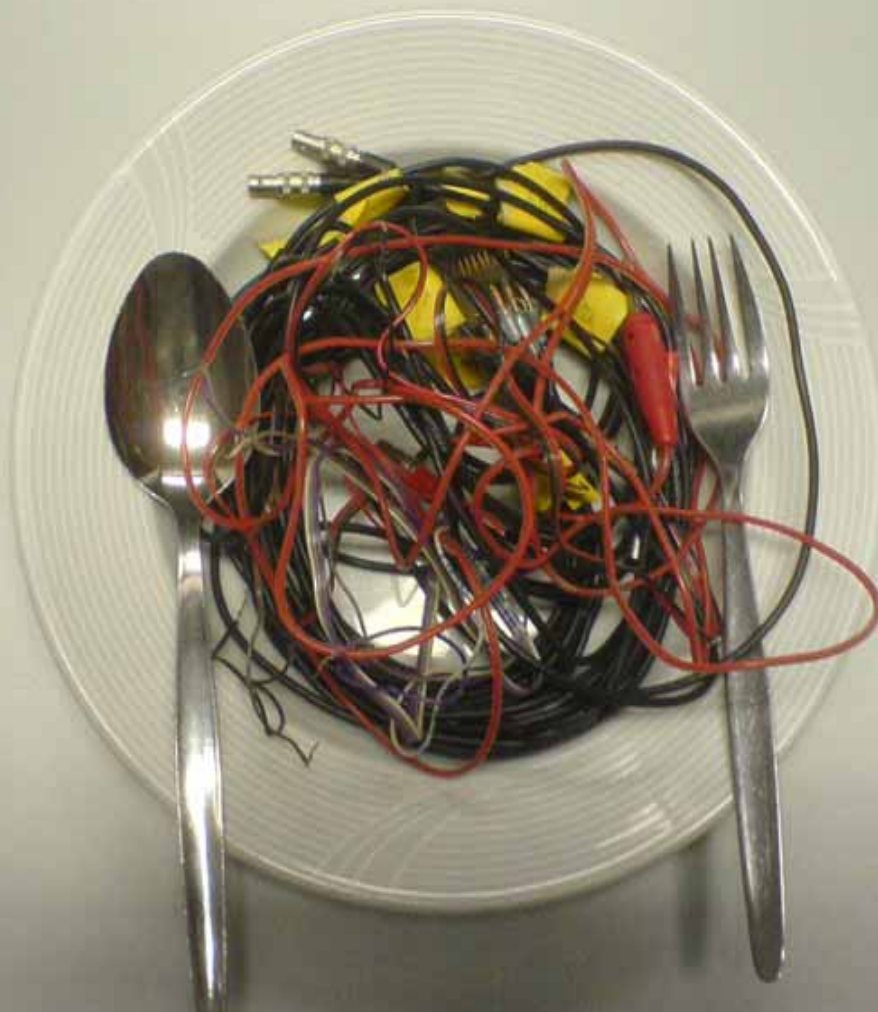
## MENU

- (i) why do we need cables
- (ii) customers aka experiments
- (iii) system integration using time stamps
- (iv) frontends
- (v) summary

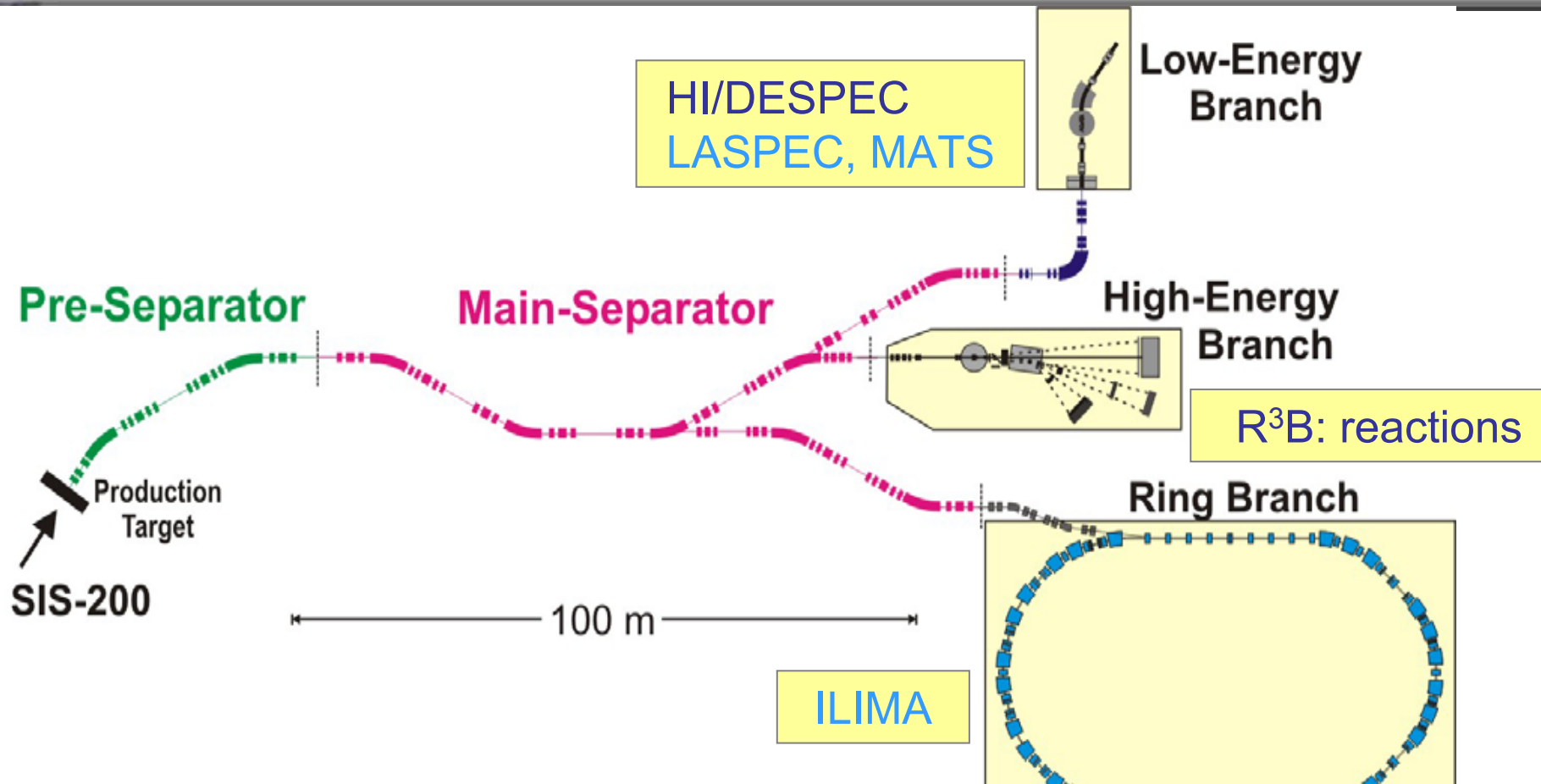
... cables !



From a few 100-1000 to half a million channels



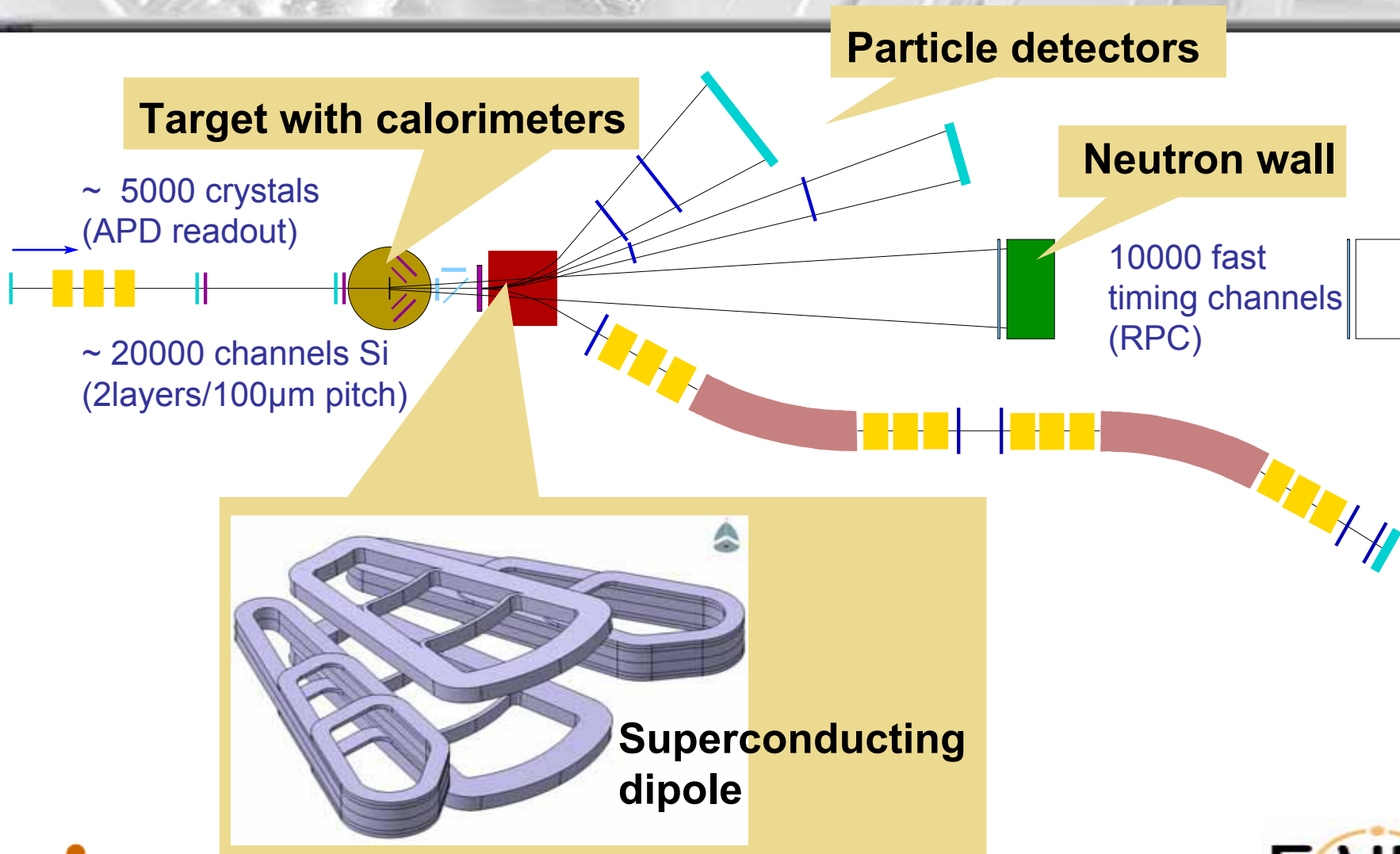
# NUSTAR Experiments (NUclear STructure Astrophysics and Reactions)



- EXL : hadron scattering
- ELISE : electron scattering
- AIC : antiproton scattering

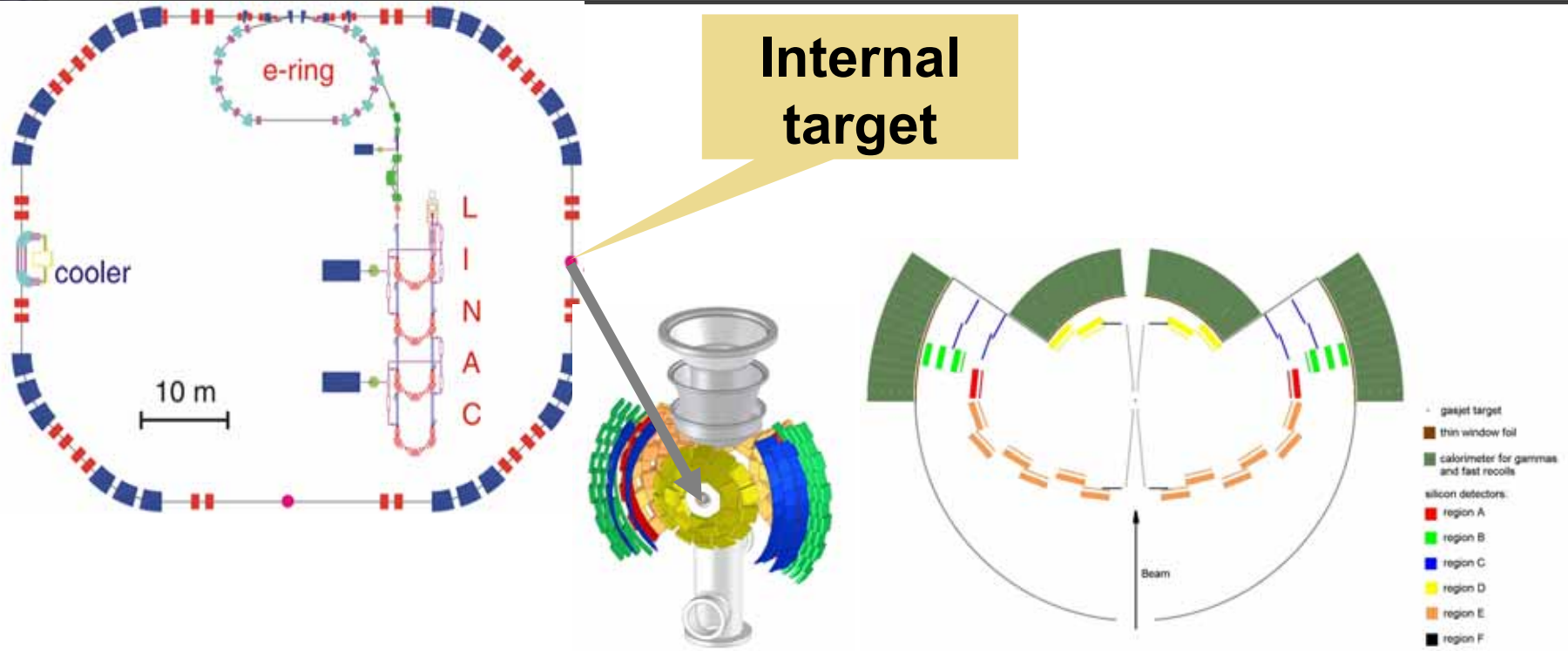
# R<sup>3</sup>B

## Reactions with Relativistic Radioactive Beams



# EXL

Exotic Nuclei Studied in Light-Ion Induced Reactions at NESR

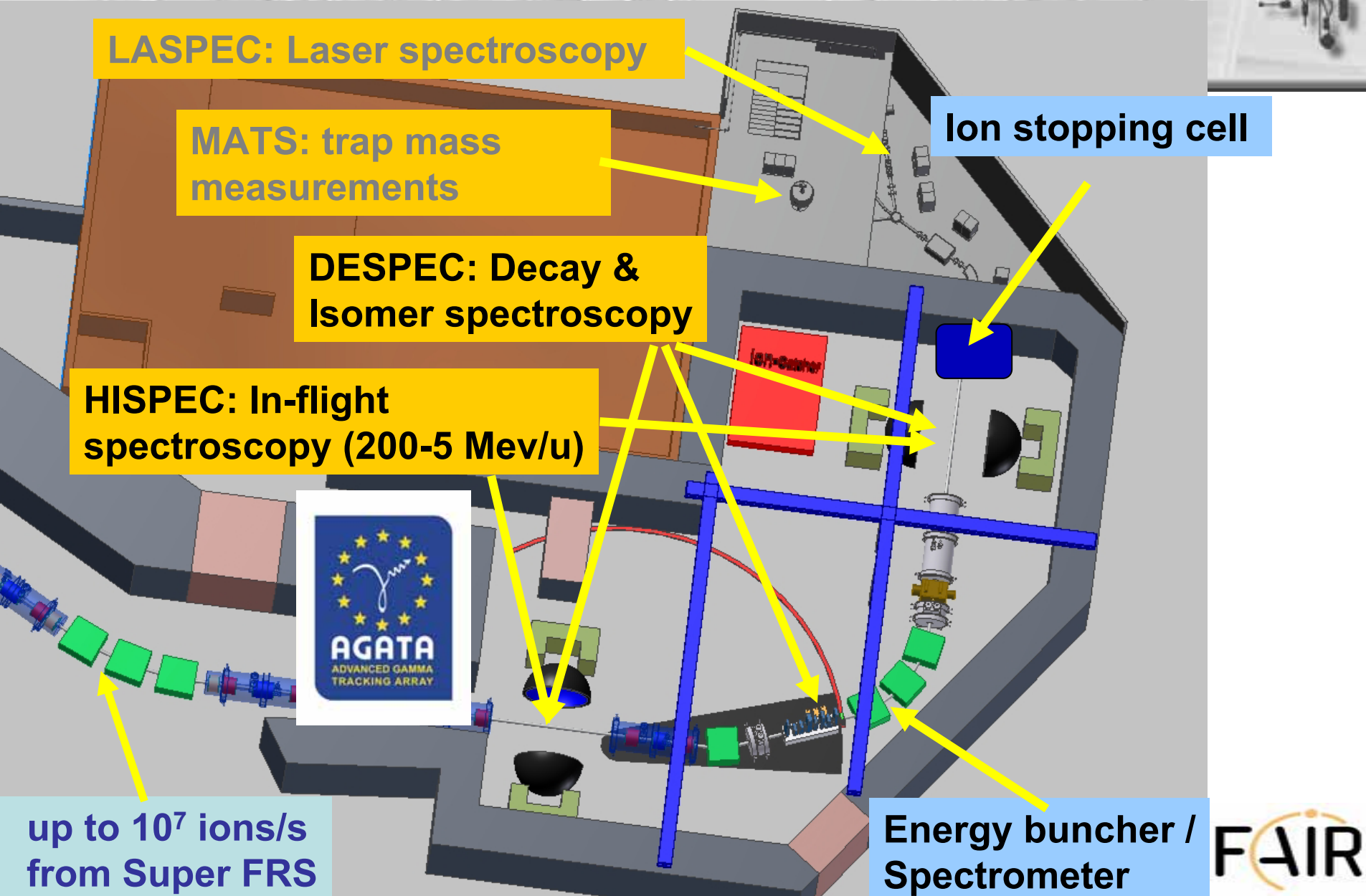


**Internal target**

## NESR

- Target-Recoil and Gamma Detector around internal target ca. 500 000 channels (Si strip, Si, CsI)
- Neutron ToF, ca. 2000 channels

# LEB: Slowed-down and Stopped beams





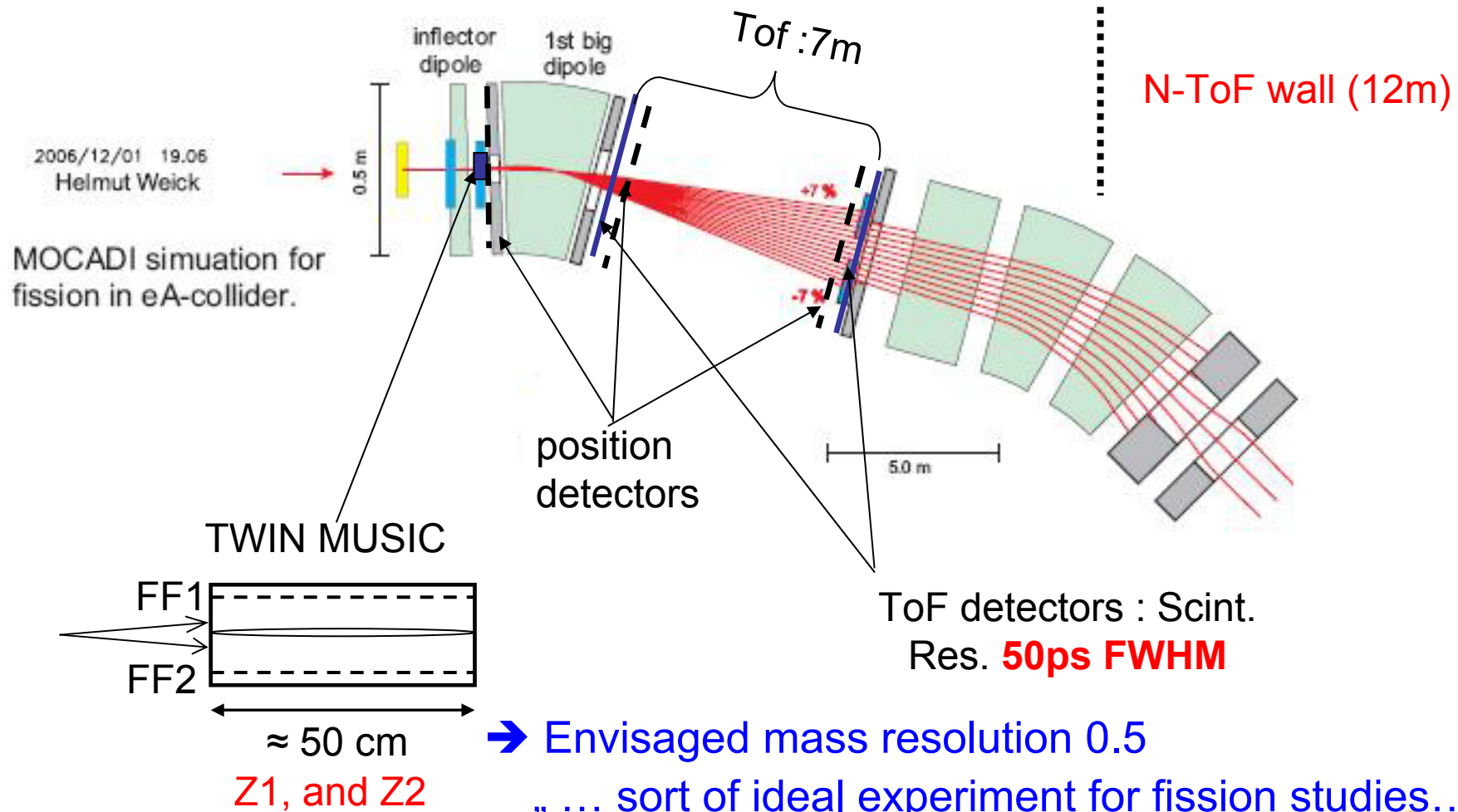
## LEB Systems:

- Agata (System Integration: Clock, Trigger, DAQ)
- Lycca (Fast timing)
- AIDA (Clock Distribution, Implantation ASIC)
- Hyde (Fully Digital Electronics)
- ...

→ FAZIA, GASPARD



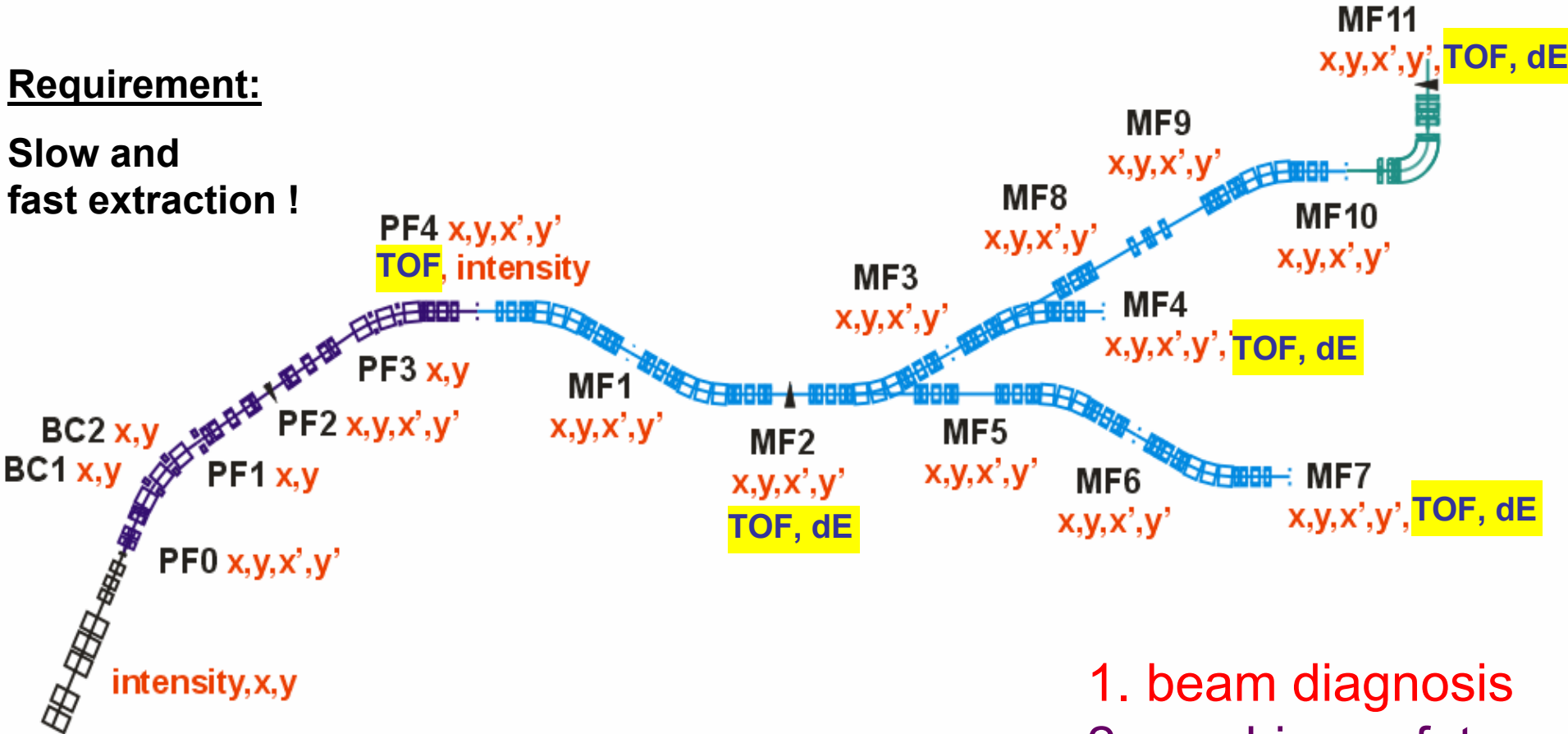
# In Ring Particle ID (AIC, ELISe, EXL, SPARC) e.g. ELISe: Experimental set-up



# Detector Instrumentation of the SuperFRS

## Requirement:

Slow and fast extraction !



1. beam diagnosis
2. machine safety
3. experiments



# B $\rho$ - $\Delta E$ -TOF method: Requirements

$$\begin{array}{l} B\rho = A/Z \cdot \beta \cdot \gamma \quad \rightarrow \quad A/Z, P \\ \text{TOF} = L/\beta \quad \rightarrow \\ \Delta E \sim Z^2/\beta^2 \quad \rightarrow \quad Z \end{array}$$

Pos res.  $\sigma \leq 1 \text{ mm}$   
Timing res.  $\sigma: 50 \text{ ps}$   
 $\Delta E$  resolution  $\sigma: 1-2 \%$

- Position: Wirechambers (single event readout)/Diamond
- $\Delta E$ : MUSIC/TEGIC
- TOF: Plastic/Diamond

**ACS/FESA**  
**DABC(MBS)/EPICS**

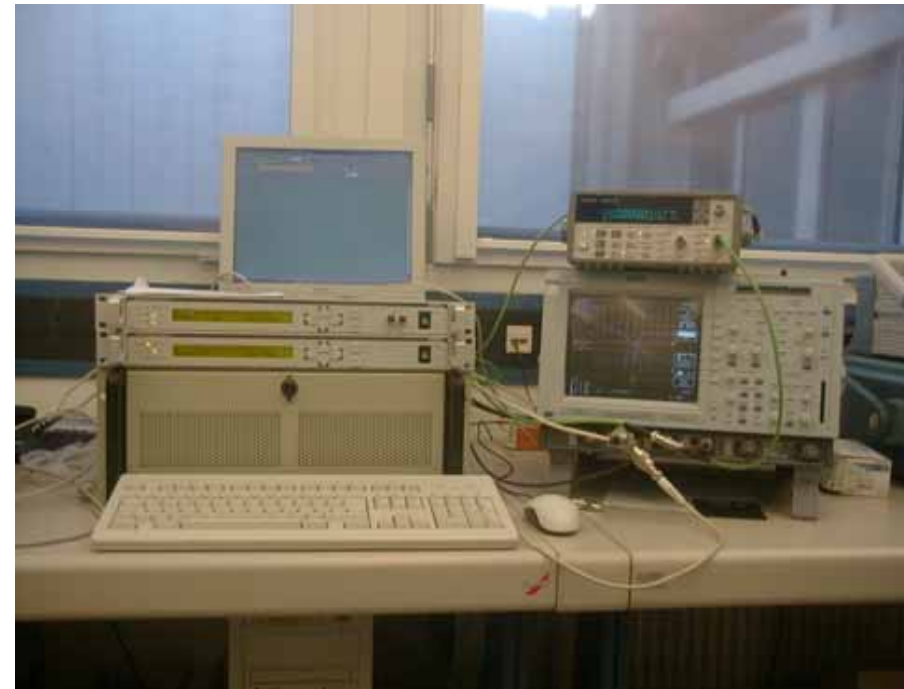
# Large Scale → Time distribution

P.Moritz (GSI)

collaboration with Works  $\mu$ -wave GmbH



- Campus wide time distribution
  - (1) Bunch timing accelerator (BuTiS) (2) Exp.: Time of flight between caves
- Synchronous local oscillators (100kHz, 10Mhz, and e.g. 200, 155 or 76 Mhz)
  - +/-100ps/km absolute uncertainty
  - few ps oscillator jitter



# BuTiS fibre distribution test bench

BuTiS Master

0.01, 10, e.g. 200 MHz copper

LASER +  
AM modulator

opt. fibre (4 \* 200GHz bands)

passive splitter  
distribution 1..2 km

Demodulator + reflector (4th ch)

0.01, 10 MHz copper

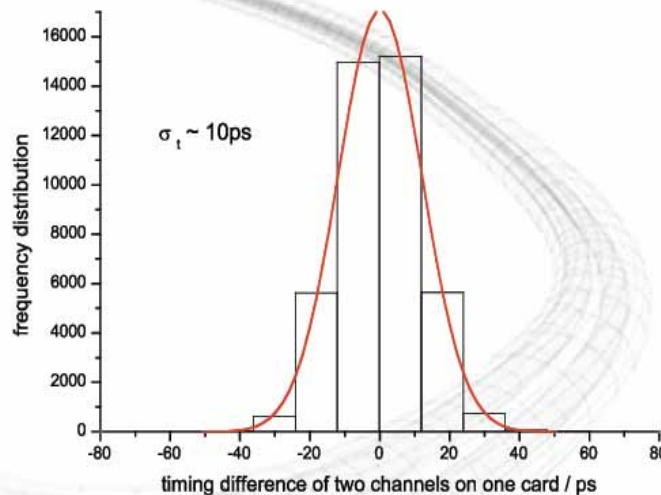
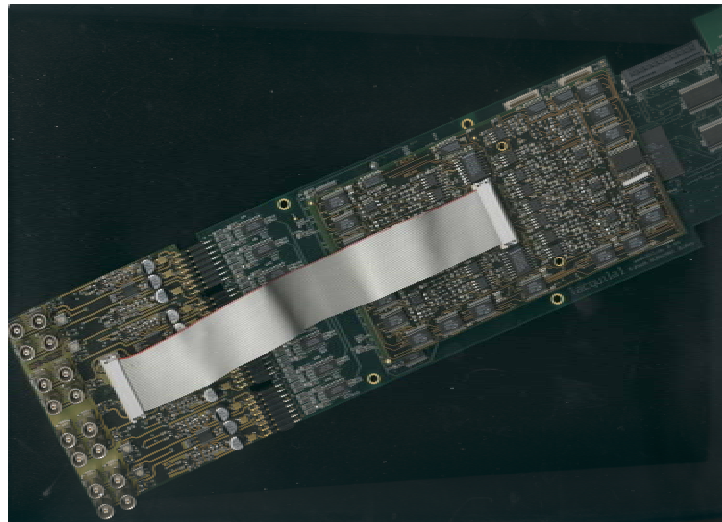
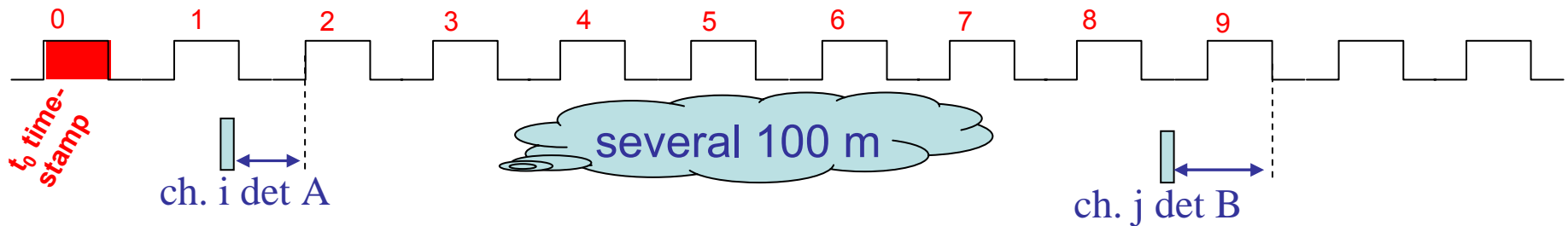
BuTiS Slave osc.

0.01, 10, e.g. 200 MHz copper → (local TDS) ?



# Precision timing (<50ps) vs. **Campus Clock**

- avoid extended cabling and dead time domains
- free running time stamped systems **SuperFRS -- Caves**



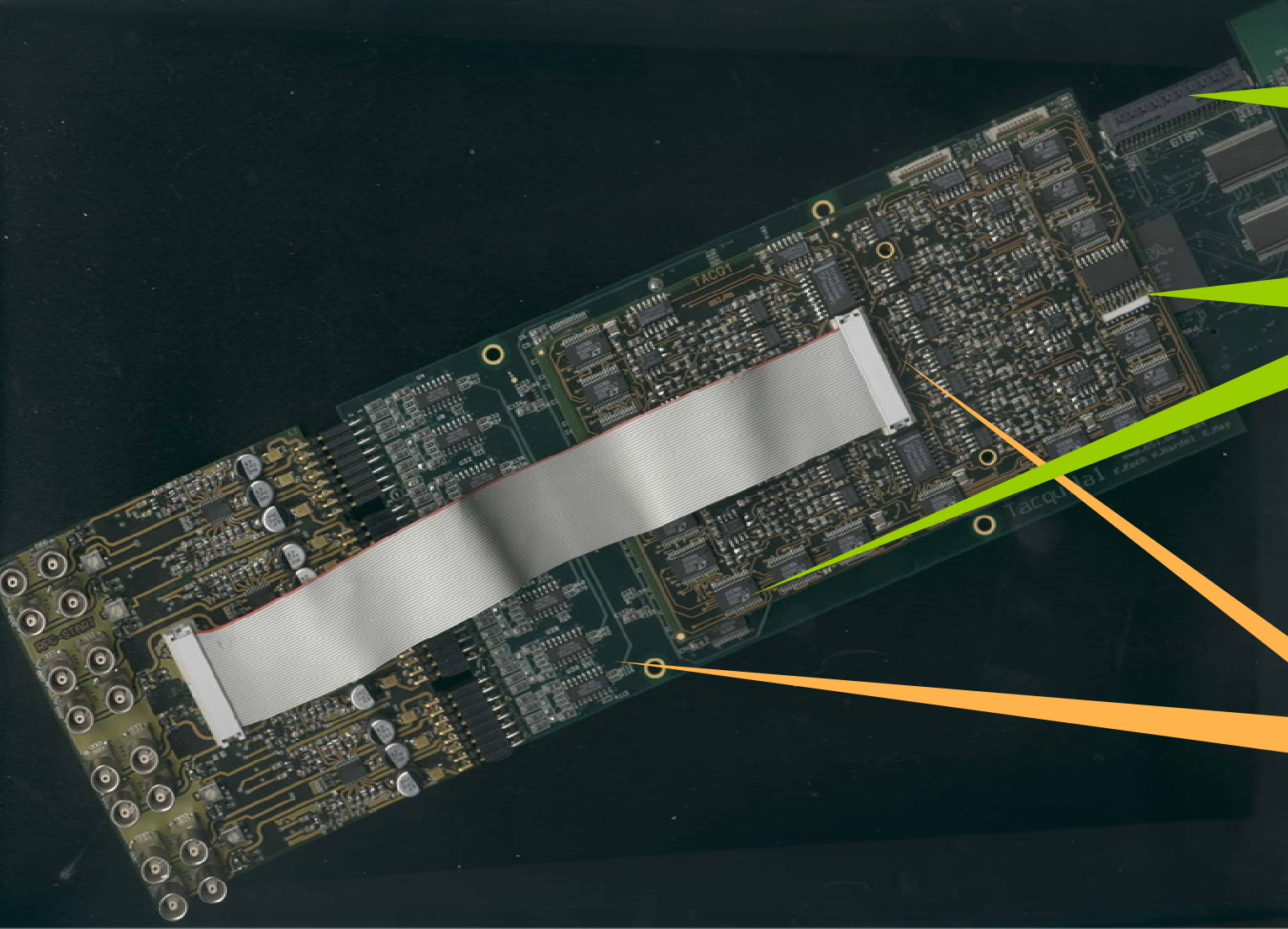
Timing FEEs:

Tacquila system  
(ASIC FhG/GSI)

New systems  
(ASIC dev. GSI)

# ASIC: Tacquila System

K.Koch, G. May, W.Ott, N.Kurz, J.Hoffmann



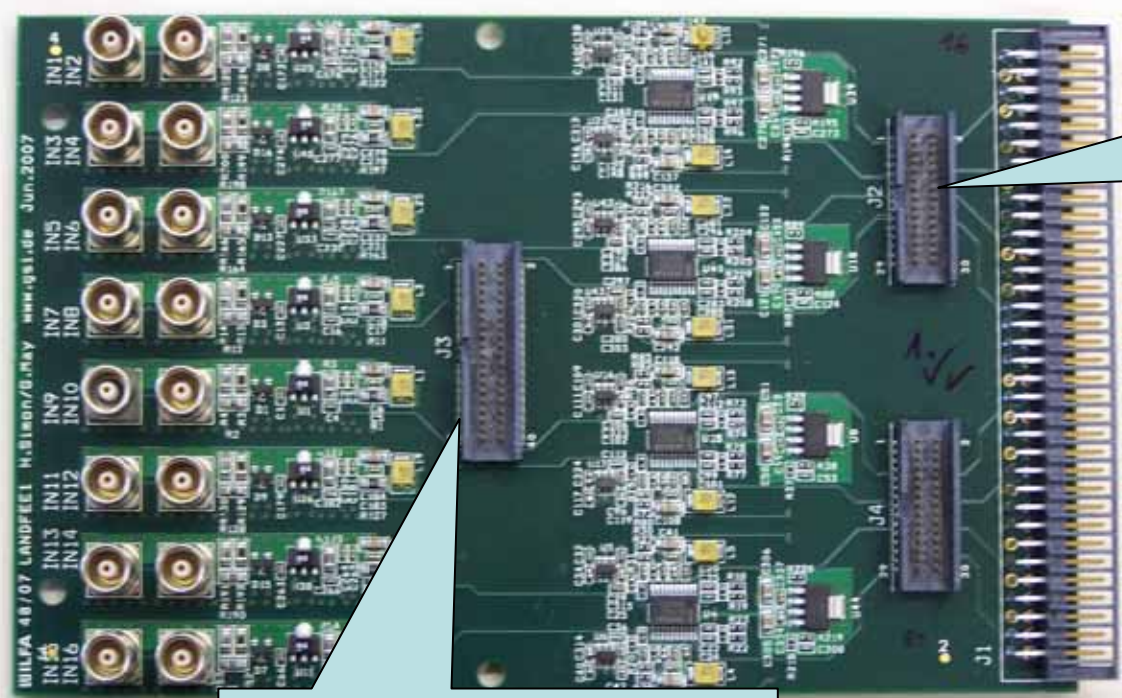
GTB interface

12 Bit ADCs  
10 Bit read ...

TAC Q uila



# New Tacquila FEE (Q1/08) → R<sup>3</sup>B-CaveC, Lycca(RISING) includes slow control, diagnostics & triggering



Comparator levels and digital interface

Analog interface (MUX, QDC, E<sub>sum</sub> trigger)

- Second board PCB design
- Piggy back close to production (I<sup>2</sup>C controls, MUX, OR, analog sum and multiplicity triggers, pulser input)



# Integration within MBS

→ synchronous or timestamped EB

Timestamps  
(TITRIS)



FE Trigger Distribution  
(TRIDI)



Trigger Module  
(TRIVA)

Logics  
Scaler/Downscale  
Deadtime locking  
Soft triggers  
(VULOM)

N. Kurz, W.Ott, J. Hoffmann



GTB & Piggy back for coupling of 'other' FEEs  
FE data transfer (Cu/LWL)  
and Processing



# TDS Systems: One clock to rule them all ...

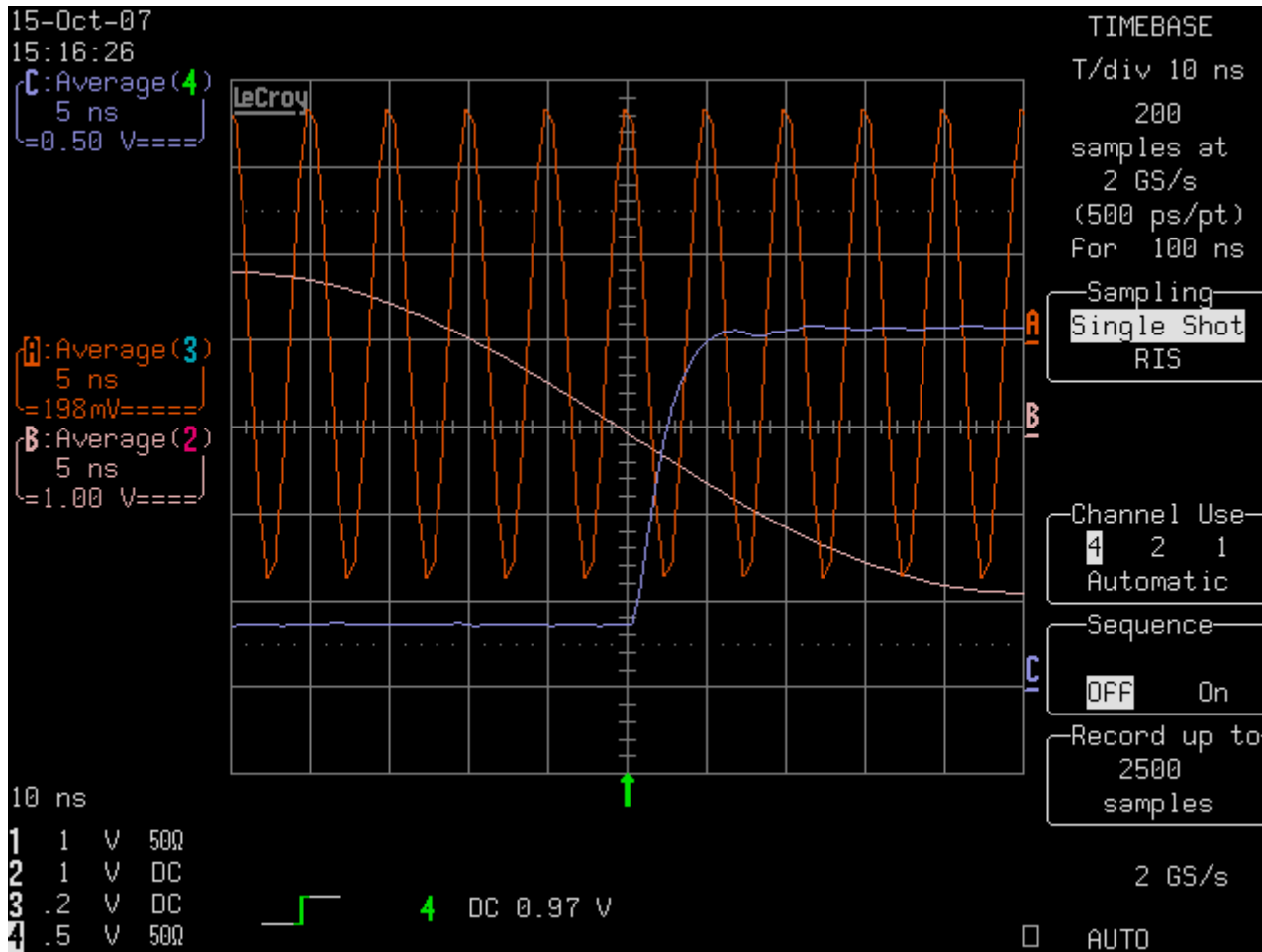
1. Coupling to existing TDS used to tag events  
(Centrum, Titris, Agava/GTS, ... )  
~ 5-10 ns separation/1ns precision

Specs. are currently prepared:

WG: J. Agramunt, M. Bellato, P. Coleman-Smith,  
N. Kurz, H. Schaffner, H.Simon

2. Precision time stamping  
~5-10 ns separation/few 10 ps precision  
→ no payload, just phase locked to TDS

# BuTiS at work (20071015)



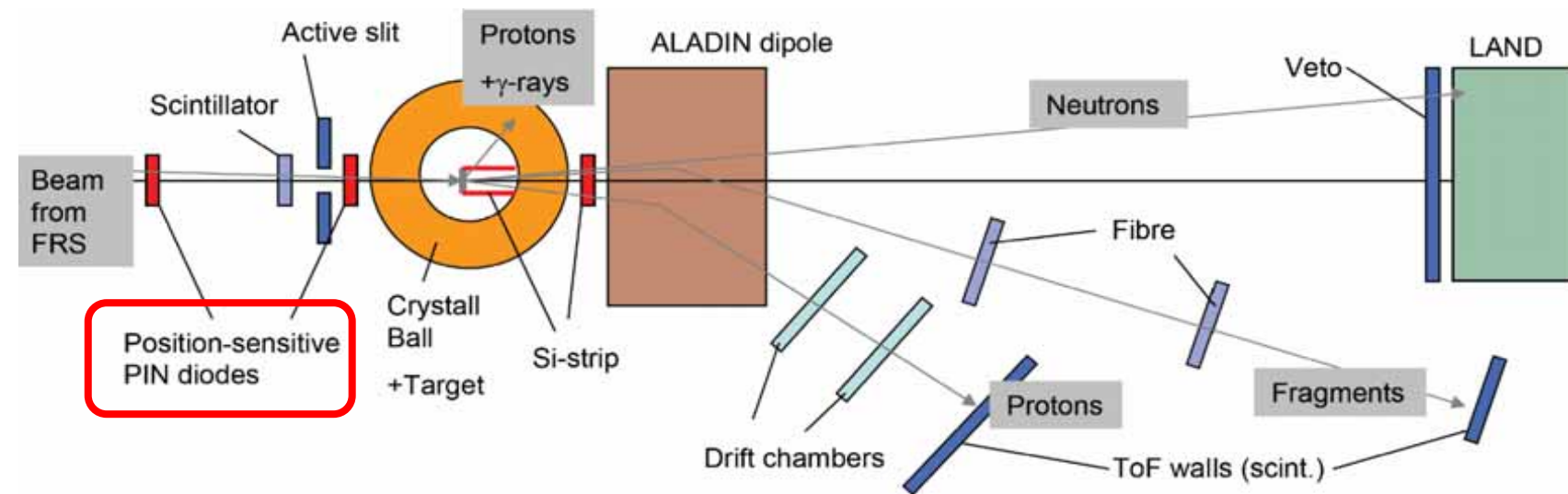
- 10, 200 MHz sine waves (adj. phase)
- T0 pulse for sync.
- very good phase stability
- BuTiS oscillator can run standalone
- about 10k€/system

# FREEDAQ: Missing building blocks

## Time Distribution:

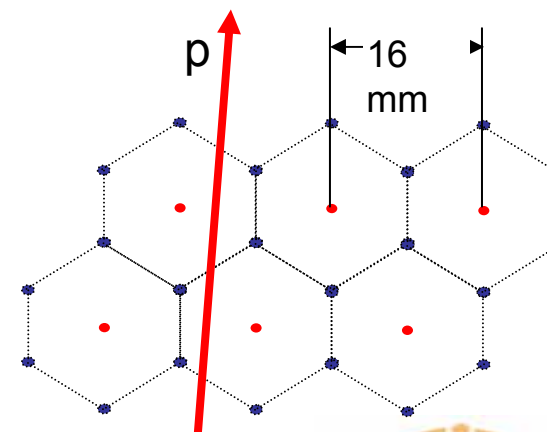
- BuTiS, anything → TDS encoder
    - intelligent triggering (few 10ps precision)
  - Experiment Wide (fibre based) distribution
    - interface to various timestamp systems
- 
- Crate Wide Distribution standard (?)
    - e.g. AIDA: 200 MHz via HDMI

# Intelligent Triggers & Controls: Test System (R<sup>3</sup>B-CaveC) Example: PSA

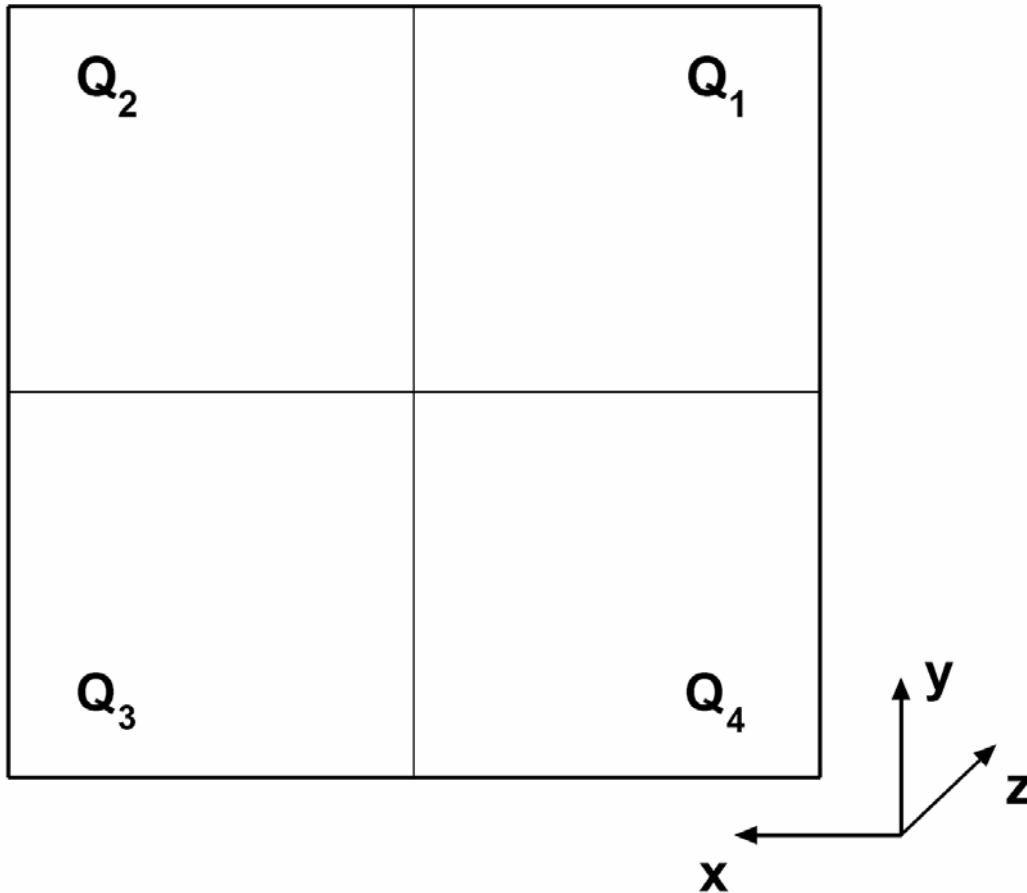


Position-sensitive  
PIN diodes

300  $\mu\text{m}$  high n-type Si  
4,5 x 4,5  $\text{cm}^2$   
B doped  $\rightarrow$  p-side



# PSP tracker



- Cathode : Sum energy
- 4 Anodes  $\rightarrow$  position

$$u = (Q_2 + Q_3) - (Q_1 + Q_4) / Q$$
$$v = (Q_1 + Q_2) - (Q_3 + Q_4) / Q$$

$$Q = Q_1 + Q_2 + Q_3 + Q_4$$

$$\rightarrow x(u, v) ; y(u, v)$$

# Idea: **Use ADC** coupled to Hades TRB2 of KVI: **Peter Schakel / Pim Lubberdink/Victor Stoica**

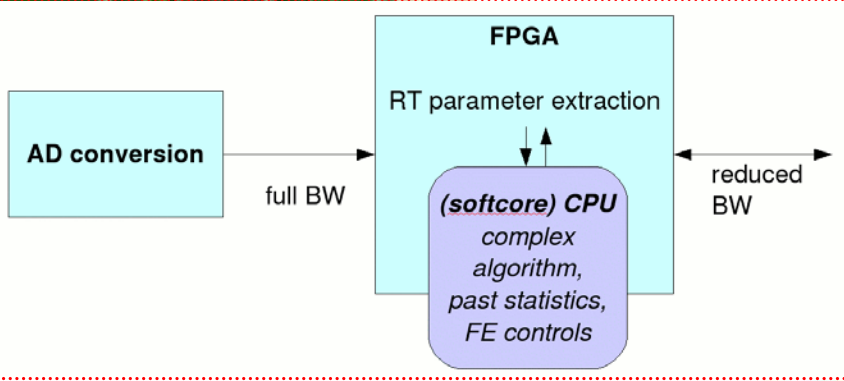
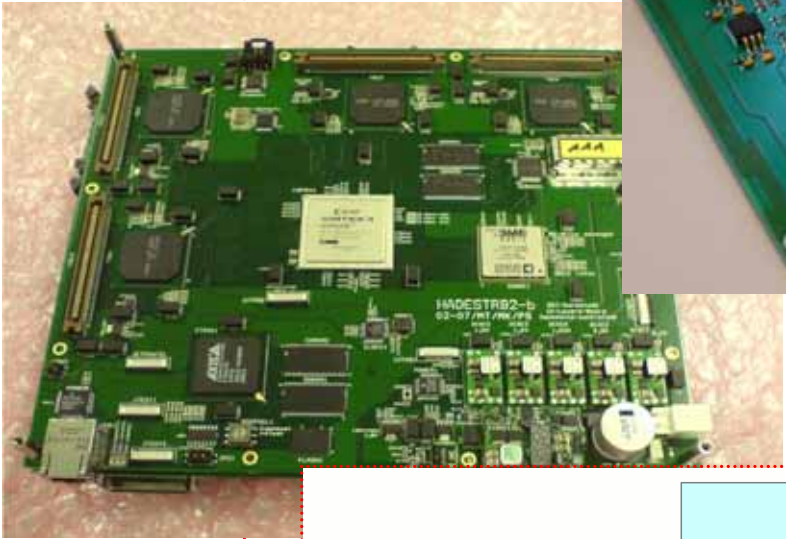


- Available hard/software environment:

- (1) ADC Piggy back / KVI  
100MS/14Bit  
50MHZ BW
- (2) Xilinx based board  
HADES TRB2
- (3) Base line follower/  
 $\kappa\sigma$  trigger

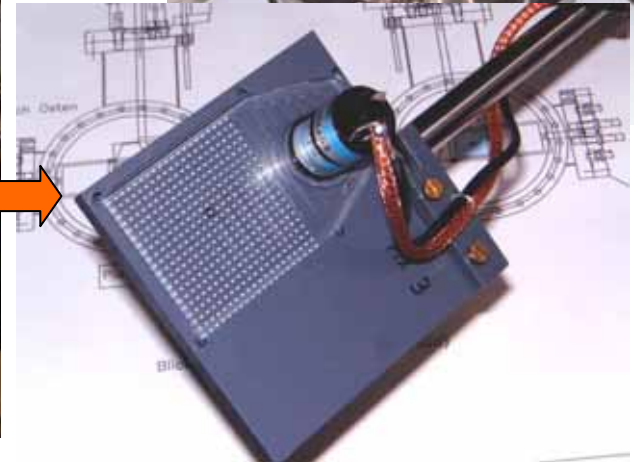
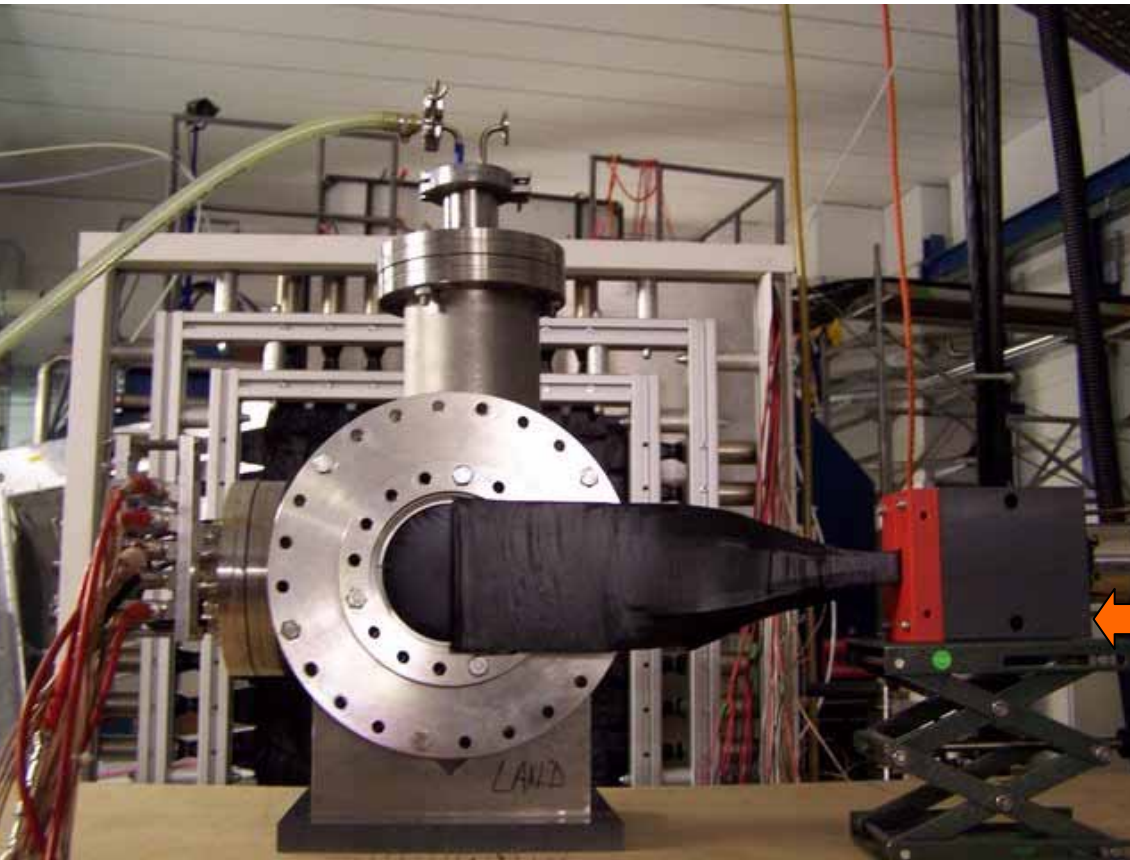
**(J. Jungmann / M. Vencelj)**

Labview based readout system



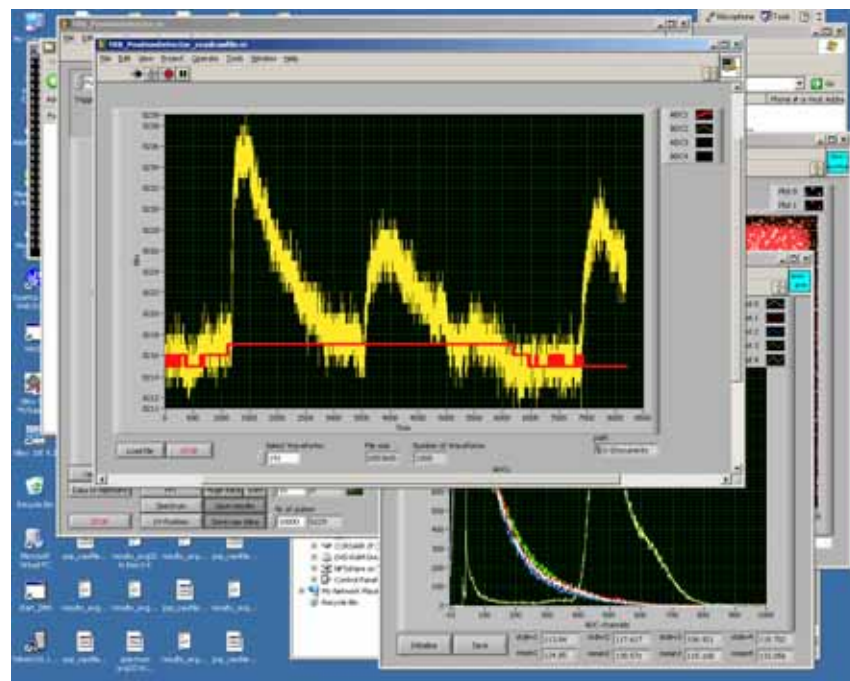
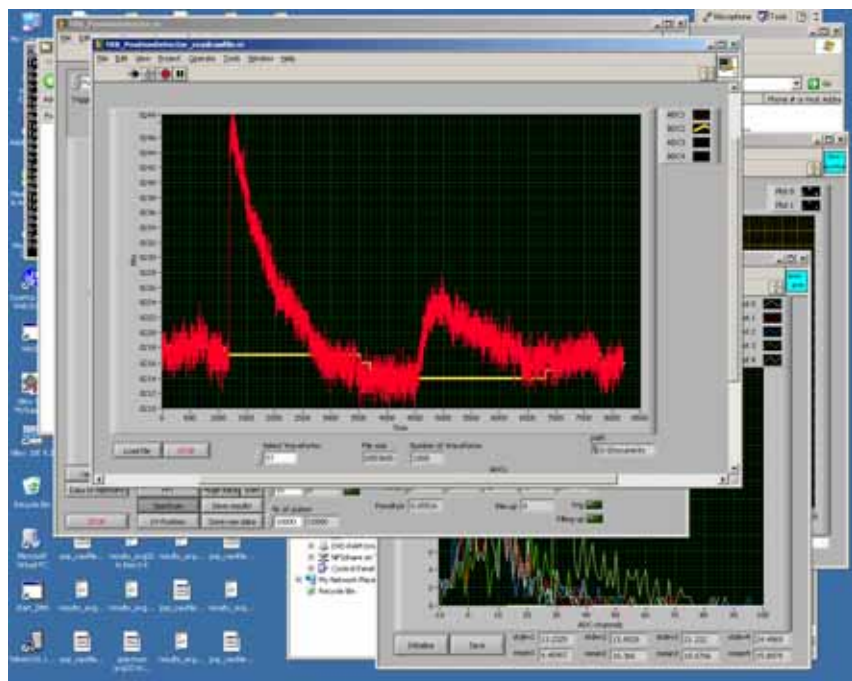
# Test experiment S327 (16.-18.4.2008)

$^{12}\text{C}$ : 550-700 MeV/u ; 2-50 kEv/s





# Results: Trigger/Baseline

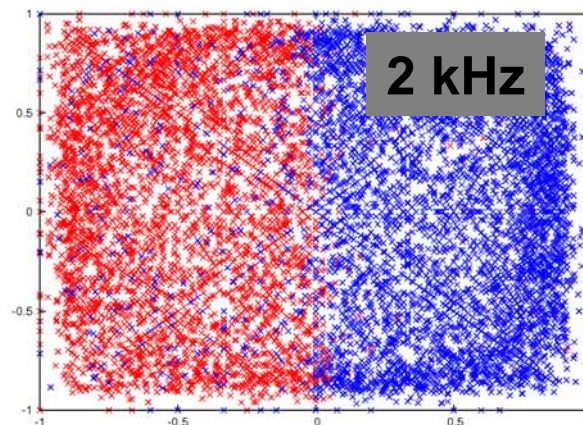
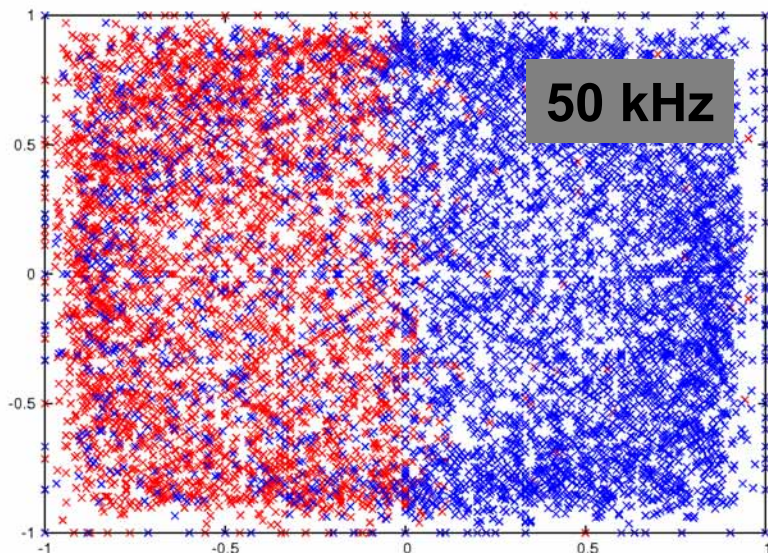


Baseline follower works !  
(Bimodal Kalman Filter)

Treatment of double hits !



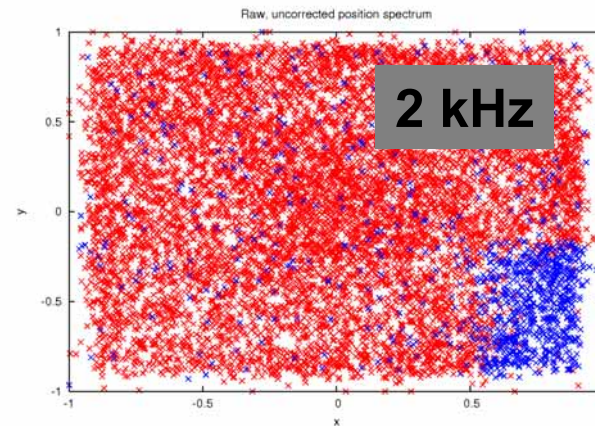
# Results: Position



Online reconstruction of positions:

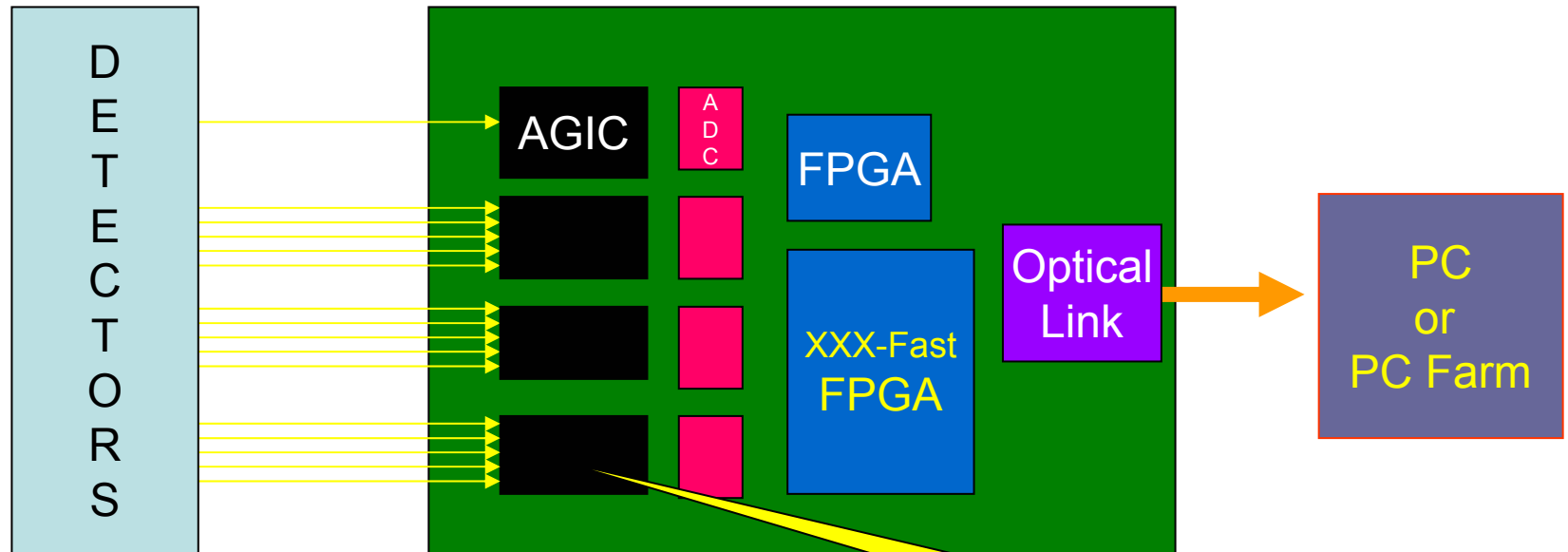
- i. @ full rate ( i.e. 50+ kHz, theoretical limit: ADC speed ! )
- ii. no correction yet

→ development of a “slow process”



# ... so what do we really want

## (c.f. FREEDAQ)

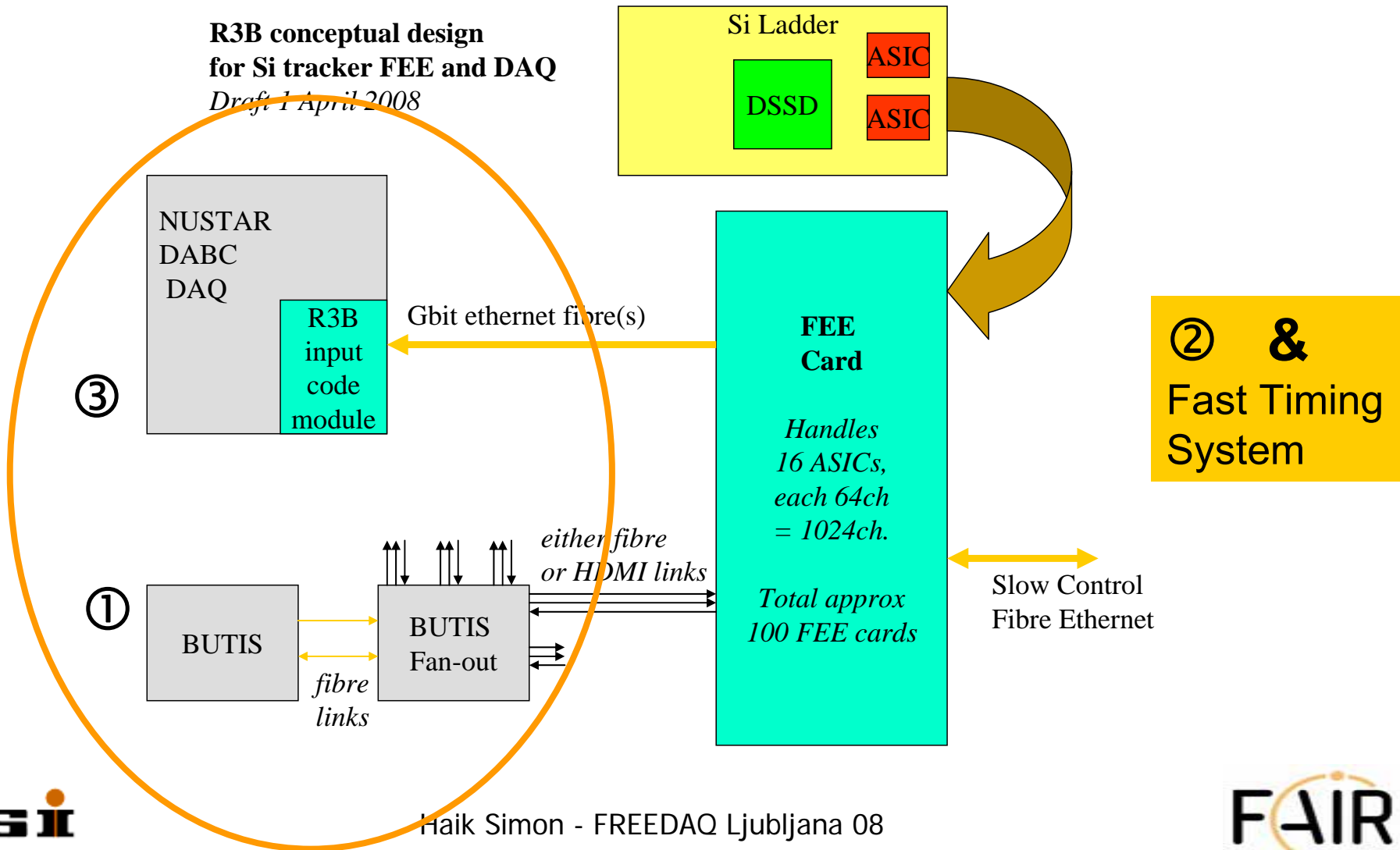


PMT, APD, PD ( $\gamma$ , n, ch. part.)  
Si(Li), DSSD, IC (ch. part: highly segmented devices)  
TPC(GEM, Micromegas, ...),

Pulse height, Q integration  
Time  
Pulse shape

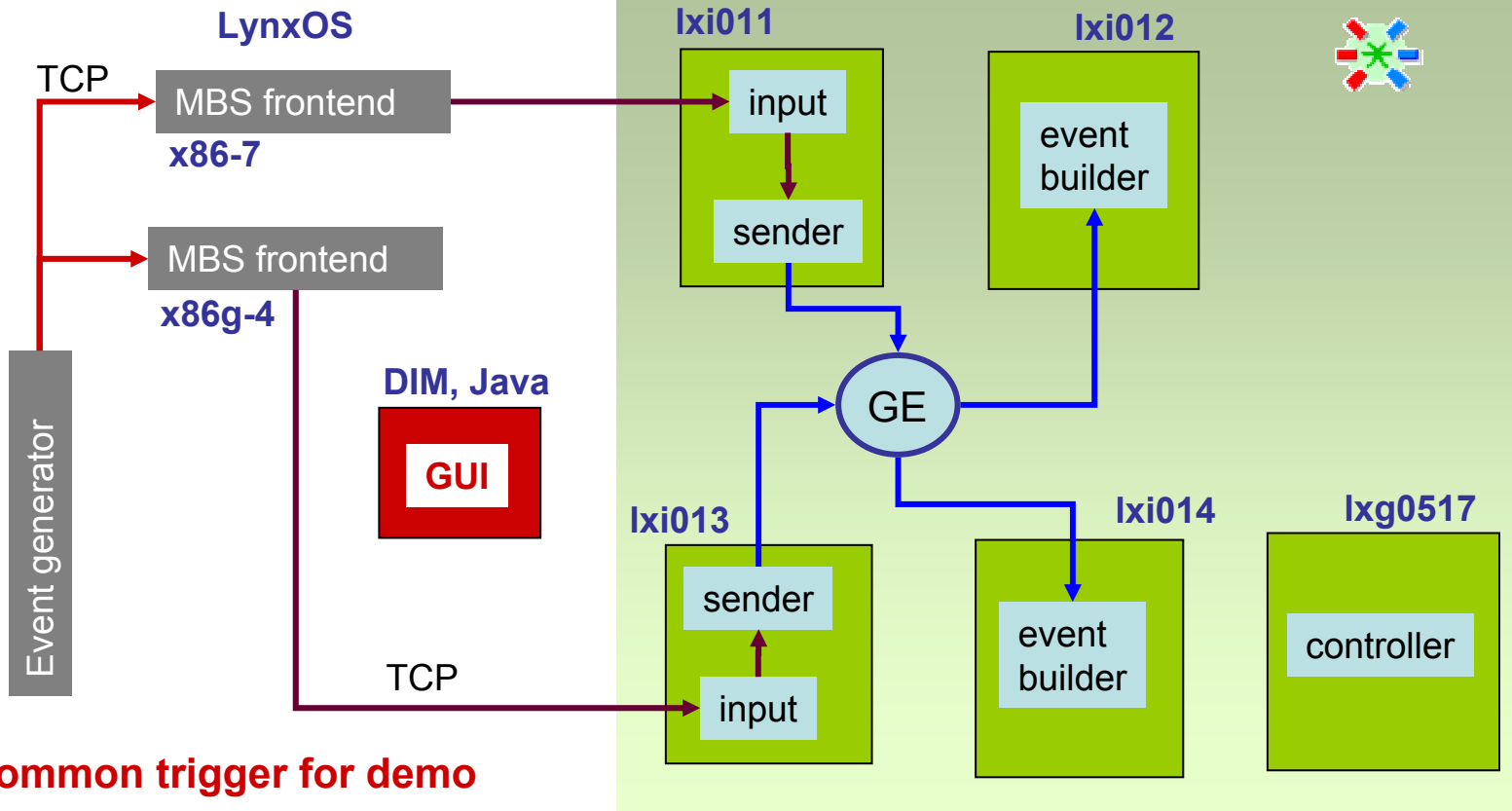
# R<sup>3</sup>B SI: Highly segmented systems ans concept for large channel counts ...

R3B conceptual design  
for Si tracker FEE and DAQ  
*Draft 1 April 2008*



# Asynchronous Collection via DABC: e.g. Network event building for MBS

N. Kurz, J. Hofmann, W. Ott



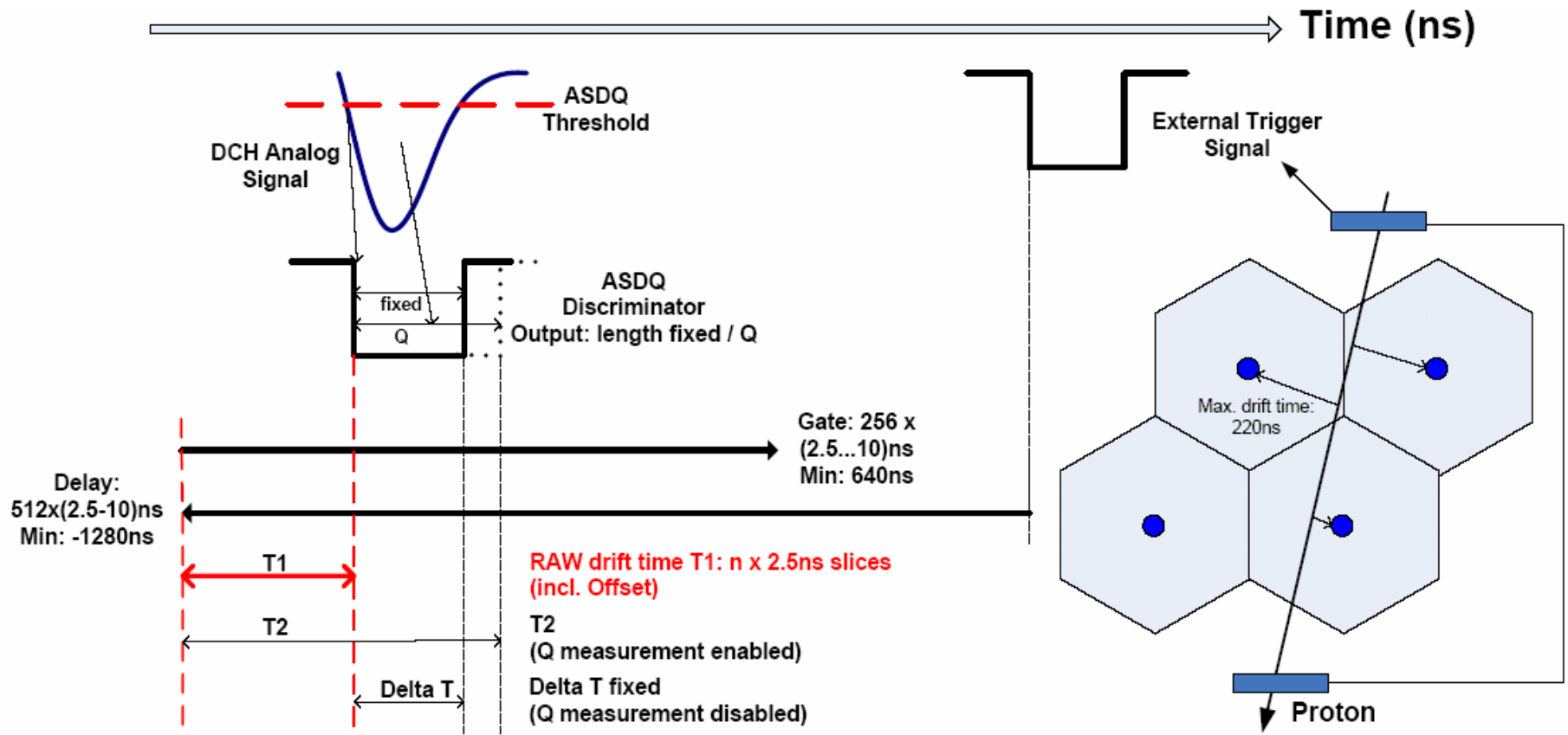
**No common trigger for demo**

GE: Gigabit Ethernet

H. Essel, J. Adamczewski, S. Linev

> DABC structure

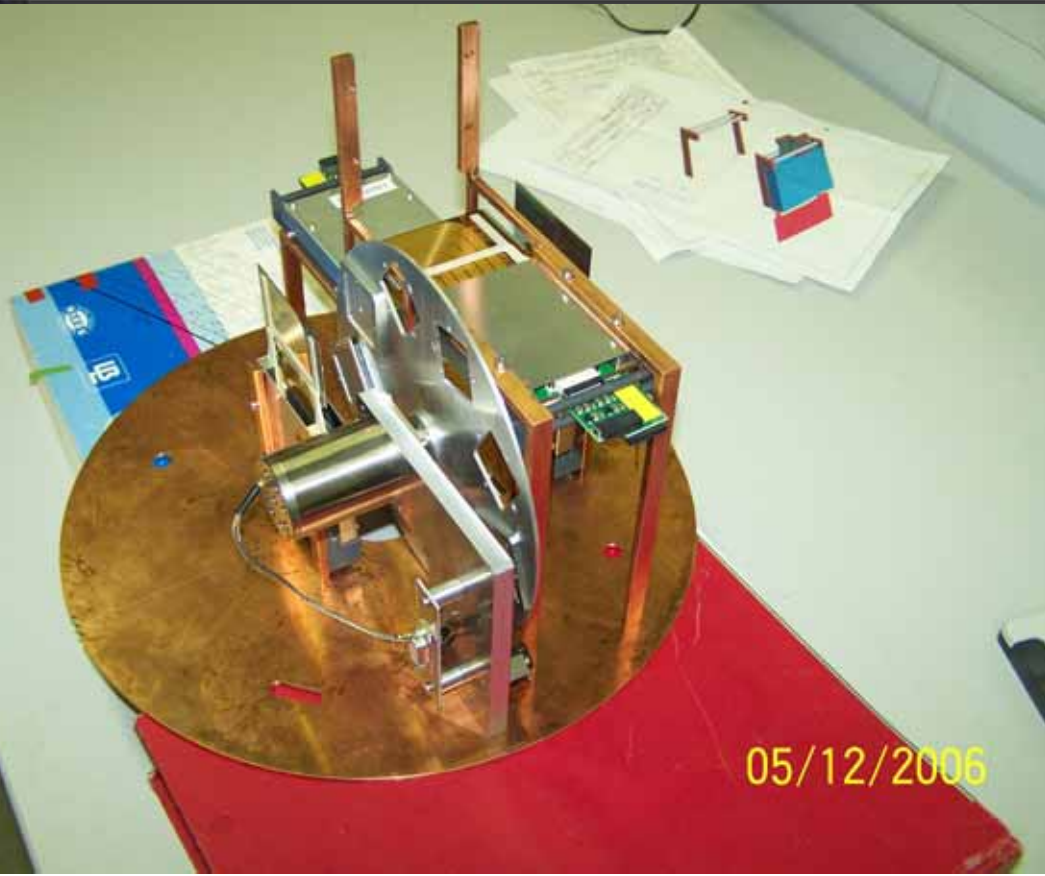
# Multichannel FEES: Timing diagramme ASDQ chip + FPGA (R<sup>3</sup>B-CaveC p-DCH)



**non collaborating !**

# R<sup>3</sup>B-CaveC Proton recoil/Ion detection in vacuum AMS/SIDEREM

**non collaborating !**



Front of the SSD (thickness 300 $\mu$ m)



41 × 72 mm<sup>2</sup> , strip pitch 100 $\mu$ m  
 Dynamic range – 100 keV - 14 MeV  
 Resolution 50keV for 5.5MeV alphas

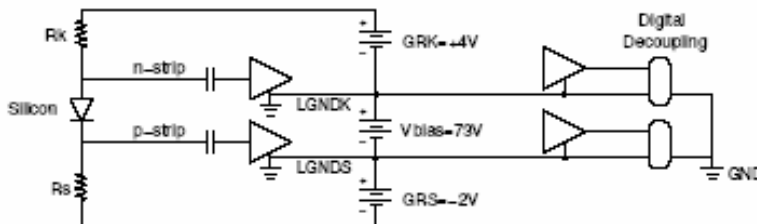
FEE

AMS(-02) readout:  
 e.g. NIM A 439 (2000) 53

6+10 read out 2\*5(320) + 6(384)  
 VA\_hdr.AMS64 resp. 9a chips  
 IDEAS/Norway → FEE: < 3W / detector

→SIDEREM (GSI/EE)

→NO self trigger/ calib. pulser !



# APV Frontend - M. Böhmer, TUM

non collaborating !



- APV25-S1 RAL  
→ CMS (Si, ...)  
(128 channel analogue pipeline  
192 columns analogue storage.  
50 ns shaped pulses  
100mV / 25,000 electrons  
40MHz sample  
Useful data marked  
test pulser, pos/neg, ...)
- I<sup>2</sup>C control
- Clck, Trg
- Low power  
consumption
- Readout to MBS  
(ADC/FPGA/DSP)



# Token Ring Scheme (NXYTER)

collaborating !

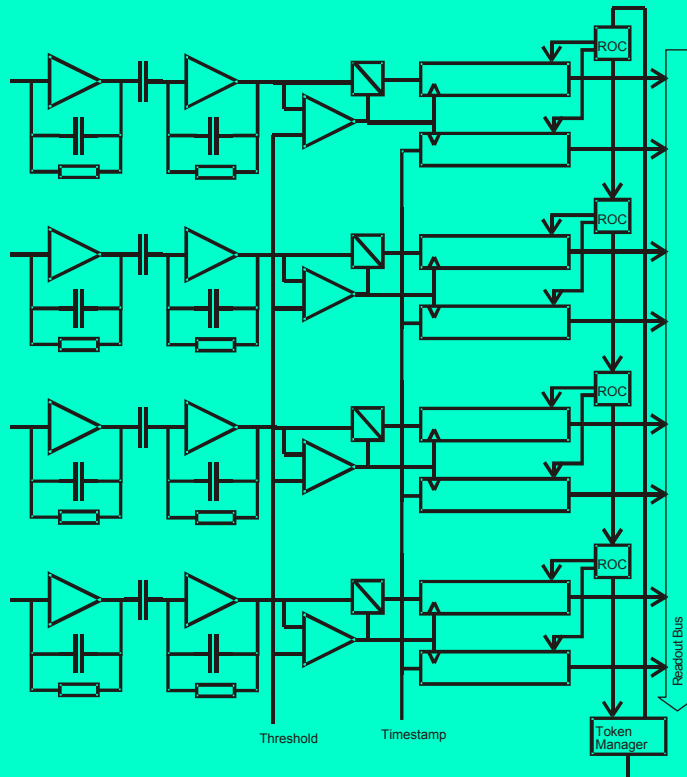


→ “deadtime free”

Ch. Schmidt (GSI)



## Sparse & derandomized readout



- Periodic readout at 20MHz
- Token asynchronously passes from channel to channel in search of data
- Within one readout cycle token could pass through all channels
- If token encounters occupied channels, data readout is initiated.
- After readout the token passes to the next channel.

→ 20 MHz/128 Ch  $\approx$  160 kHz

**ENOB 10.4**

Ulrich Trunk  
Physikalisches Institut der Universität Heidelberg



Variety of applications: Test with single wire readout foreseen !



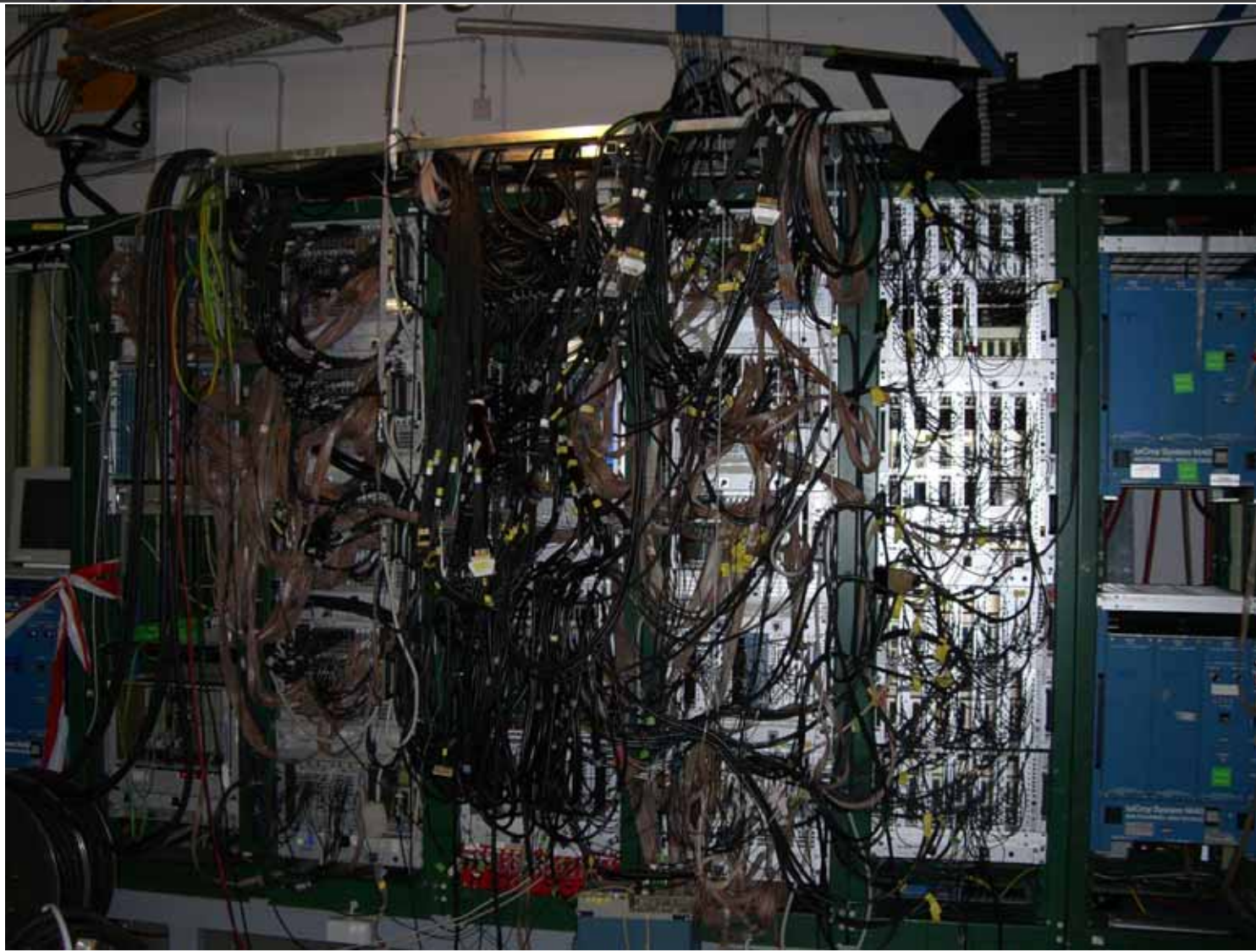
# Summary

- System design studies
- FEs either integrated into existing (DAQ/controls) infrastructure
- ... or handled software wise (DABC)
- Missing (FREEDAQ) Items
  - timestamp distribution and protocol
  - adequate multi-channel FEs with high dynamic range



**FIN**

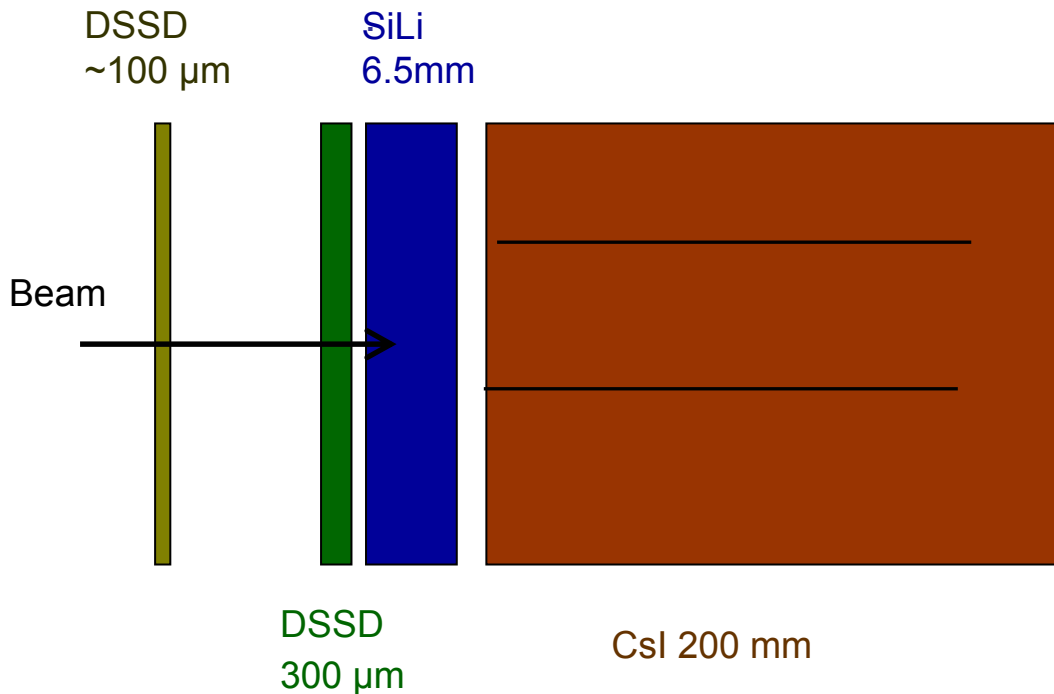
**LAND electronics ~600 ch 7  $\rightarrow$  1 +  $\epsilon$  crates !**



= 30 Tacquila cards with LAND FEE + 2 VME helper modules + 1 VME CPU + 10 VME QDCs + 3 HV bins

# Common Demonstrator Layout

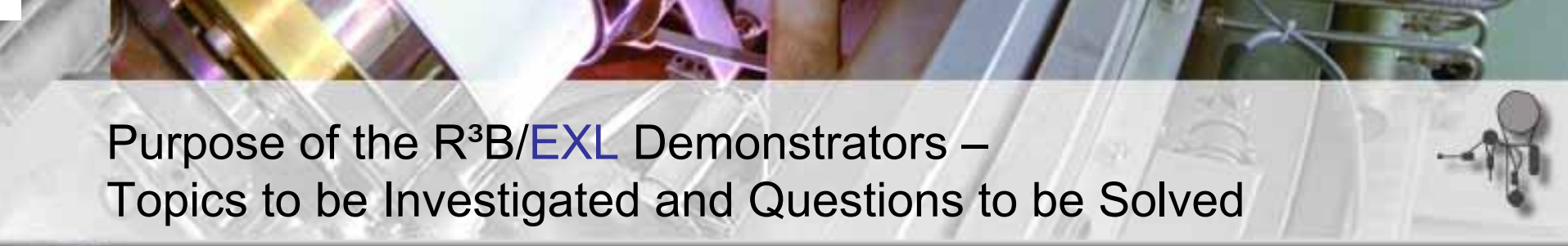
R<sup>3</sup>B, EXL, others (?)



- modular
- vacuum compatible
- readout ?

( self triggerable,  
test/calib. facilities,  
high dyn. range,  
time stamps ... )

First DSSD – e.g. 2.1 x 2.1 cm<sup>2</sup>, 0.3/1.25 mm pitch (PTI, EXL) or 0.1/0.1 mm pitch R<sup>3</sup>B  
Second DSSD – e.g. 5.2 x 6.7 cm<sup>2</sup>, 0.1/0.2 mm pitch (Micron, EXL) or 0.1/0.1 mm pitch R<sup>3</sup>B  
Si(Li) or Si – e.g. 9 x 5 cm<sup>2</sup>, 4 x 2 pads ---- EXL  
Csl – e.g. volume 3 x 3 cm<sup>2</sup> x 20 cm



## Purpose of the R<sup>3</sup>B/EXL Demonstrators – Topics to be Investigated and Questions to be Solved

- Detection of MIP`s with thin DSSD`s
- Tracking with high resolution
- Performance of CsI in combination with Si detectors
- Energy and position resolution for protons, alphas for various energies
- Performance of DSSD`s with larger pitch size ( from 0.3-1.5 mm )
- Very low threshold detection
- PSA
- Combination of DSSD`s with Si(Li)`s
- Vacuum compatibility
- Heat production
- Feedthroughs
- Noise Analysis
- Evaluation of realistic background conditions
- Definition of demands for the final ASIC design

## Possible Design of the Demonstrators

- **frames and readout boards:**

should be common for EXL- and R<sup>3</sup>B demonstrators

should be made from ceramics

potential producers are PTI, Mesytech, Uppsala, India

the design of MUST could be a basis

responsible for design and construction: O. Kiselev, H. Simon

- **readout:**

number of readout channels: around 1000, frontend in (high) vacuum

(for EXL: bakeable to at least 150 °C see CHICSI setup)

trigger: external trigger → self triggerable

dynamic range: 150 keV – 5 MeV ( in Si(Li) up to 100 MeV)

data rate: 1-10 kHz

options: Jülich, Daresbury, AMS, GSI nXYTER

responsible for readout: R. Lemmon, O. Tengblad, P. Golubev

# Detector Scheme for Super-FRS target area

available/possible systems

## Fast extraction

Resonance Transformer

Diamond

(single crystal, current readout)

Pickups

Beam induced fluorescence(BIF)

Rest Gas Monitor (RGM)

Current Grids

Camera on target (IR)

## Intensity

## Position

## Profile

## Monitoring

## Slow extraction

Cryogenic Current Comparator  
(SQUID)

SEETRAM

Diamond (poly crystal & particle)

BIF

RGM

Current Grids/Wire chambers

Camera on target (IR)

*full intensity* | *reduced intensity (< about 1 nA)*