The readout of the Si-detectors consists of the following parts:

Inside vacuum:

Si-detector with "spring pin" connectors

Cable from Si-detector to Capacitor intermediate PCB

Capacitor intermediate PCB for AC coupling of the signals

Eight 34-wire ribbon cables between Capacitor intermediate PCB and VA-TA ASIC PCB

VA-TA ASIC PCB:  ‘testing board for demonstrator designs’ with 8 VA-TA ASIC’s

Cooling for VA-TA ASIC PCB including the cables

Ribbon cable and shielded 2-wire cable from VA-TA ASIC PCB to Flange feedthrough connector

Flange feedthrough connector

Outside vacuum:

Cable from Flange feedthrough connector to VA-TA interface board

VA-TA interface board, with LVDS – ‘bipolar digital’ converters and voltage regulators

Two 68 pins from VA-TA interface board to VUPROM FPGA VME board

VUPROM FPGA VME board

Shielded 2-wire cable from Flange feedthrough connector to ADC VME board

ADC VME board: CAEN V550

Status:

The VA-TA ASIC testing board for demonstrator designs is being produced. The PCB will arrive in 2 weeks. The layout is attached.

The VA-TA interface board is also being produced and will arrive in week 44.

Schedule:

Ordering cable Ribbon cable and shielded 2-wire cable from VA-TA ASIC PCB to Flange feedthrough connector: week 44 (Peter Schakel)

The soldering of the components on the VA-TA interface board: week 44/45 (KVI)

Testing of the VA-TA interface board: week 45/46 (KVI, Michel Hevinga)

The soldering of the components on the VA-TA ASIC board: week 46/47 (KVI)

Testing of the VA-TA ASIC board: week 47/48 (KVI, Michel Hevinga, Peter Schakel)

Next to be done:

ASIC bonding on the PCB by GSI: Matthias Holl and Carmen Simons (probably first one ASIC-set, and after testing the other 7)

Writing FPGA code for the VUPROM and Software for the CAEN ADC board: Matthias Holl.

Testing of the ASIC’s with realistic signals: GSI, Matthias Holl

Mechanical design of the VA-TA ASIC PCB and cable cooling: KVI, depends on specification of the Capacitor intermediate PCB and the cables (Brano Streicher).

Design and fabrication of the Capacitor intermediate PCB (see ‘To be discussed’)

To be discussed:

Cable from Si-detector to Capacitor intermediate PCB. Position and layout of the Capacitor intermediate PCB. Brano Streicher and Oleg Kiselev will organize a video conference in week 44.

Flange feedthrough connector : KVI